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EE323: Microprocessor Systems Design
Final Exam Solution (1h30)
2019 – 2020

Notes: Answer briefly and clearly using the provided space. No extra sheet will be accepted.

1. Z80 Program Execution (8 pts)

Consider the simple program given in Table 1.

1.1 Give the number of M-cycles, memory read, and memory write cycles of the program.

The number of M-cycles: 13
The number of memory read cycles: 6
The number of memory write cycles: 1 *(1 pt)*

1.2 Assuming 4 MHz clock frequency, give the execution time of the program.

Clock period = 1/(4MHz) = 0.25 µs
The number of T-states: 45
*Execution time = 45 * 0.25 = 11.25 µs* *(1 pt)*

1.3 Give the value on the data and address bus during the execution of the `SUB B` instruction.

Z80 inserts $\overline{RD}$ signal during the fetch cycle of the SUB B instruction
The HEX value on the address bus = address of the instruction = 2347H
The HEX value on the data bus = opcode of the instruction = 90H *(1 pt)*

1.4 Give in decimal the available size for the stack.

SP = 3FB0H
The Address of the HALT instruction = 234BH
Available locations = (3FB0H-1) - (234B+1) + 1 = 1C64H = 7262 locations
Available size = 7262 Bytes *(1 pt)*

1.5 Give the content of registers A and B after the execution of the `SUB B` instruction.

B = B9H
A = A9H – B9H = A9H + 47H = F0H *(1 pt)*

1.6 Give in decimal the operation executed by the `SUB B` instruction in case of: a) unsigned numbers, and b) signed numbers.

We have A = A9H - B9H = F0H
a) A = 169-185 = 240 (result is false --> carry flag = 1) *(1 pt)*
b) A = (-87)-(-71) = -16 (result is correct --> overflow flag=0, sign flag=1) *(1 pt)*

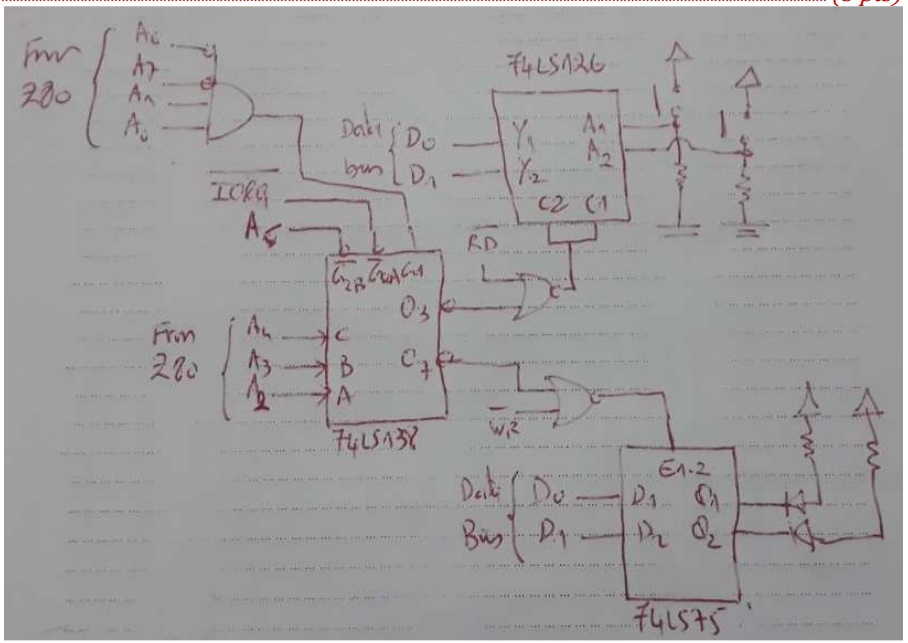
1.7 Give the status of the Carry, Sign, and Overflow flags after the execution of the `SUB B` instruction.

Carry flag = 1
Sign flag = 1
Overflow flag = 0 *(1 pt)*

2. Z80 I/O Interfacing and Assembly Program (7 pts)

2.1 Using full address decoding, design a circuit to interface to Z80 two active high push-buttons (B0 and B1) with port address 0FH and two common anode LEDs (L0 and L1) with port address 1FH. You should use 3-to-8 decoder (74LS138), Quad 3-state buffer (74LS126), Quad Latch (74LS75), and basic logic gates.

(3 pts)



2.2 Write a program to continuously read the push-buttons and if the two buttons are pressed, it turns on the LED L0 for 2 seconds and then the LED L1 for 2 s (we assume that we have a 2 s delay subroutine stored at memory location 3000H).

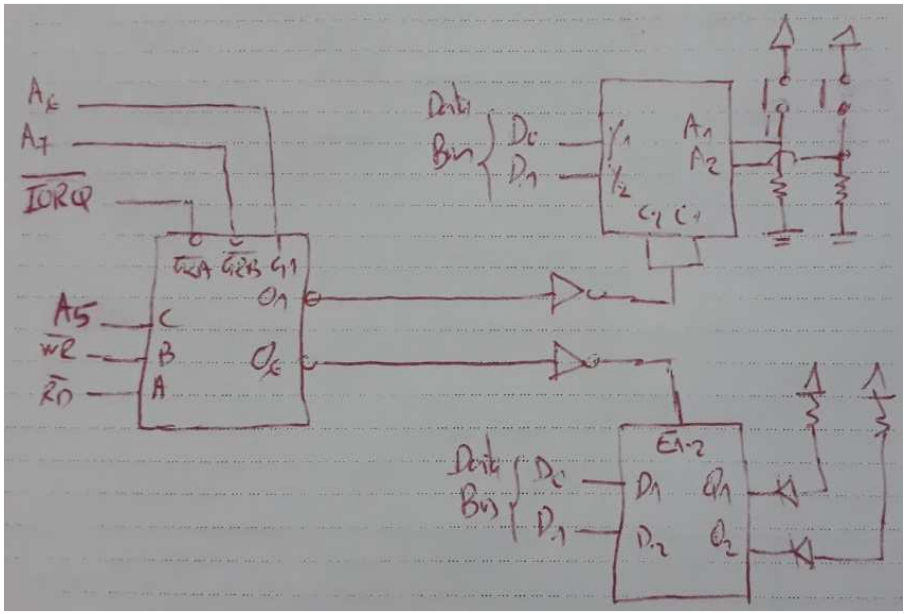
(3 pts)

No	*Instruction*
	`.ORG 2000H`
1	`START: LD SP, 3FB0H`
2	`LOOP: IN A, (0FH)`
3	`RRA`
4	`JR NC, LOOP`
5	`RRA`
6	`JR NC, LOOP`
7	`LD A, 02H`
8	`OUT (1F), A`

No	*Instruction*
9	`CALL 3000H`
10	`LD A, 01H`
11	`OUT (1F), A`
12	`CALL 3000H`
13	`LD A, 03H`
14	`OUT (1F), A`
15	`JR LOOP`
16	
17	

2.3 Propose a new design to interface the 2 switches and 2 LEDs using partial decoding with only one 3-to-8 decoder, 3-state buffer, latch and inverters (without using any other gate).

(2 pts)



2.4 Give the used port address for the LEDs and for the push-buttons.

Port address for push-buttons: 010X XXXX (e.g. 40H)
Port address for LEDs: 011X XXXX (e.g. 60H) *(1 pt)*

3. Z80 Memory Interfacing (5 pts)

Consider a Z80 system with two SRAM memories 16 KBytes and 8 Kbytes. The 16 KBytes is interfaced using linear address decoding (A14=1) and the 8 Kbytes is interfaced using full address decoding.

3.1 What is the total used space? Give the memory map for the 16 Kbytes memory.

*Total used space: 2*16 Kbytes + 8 Kbytes = 40 KBytes*
Memory map: Memory range: 4000H-7FFFH
Foldback range: C000H-FFFFH

3.2 Give Z80 instructions to load the value 9FH into the first memory location of the 16 Kbytes memory using immediate 16-bit pointer.

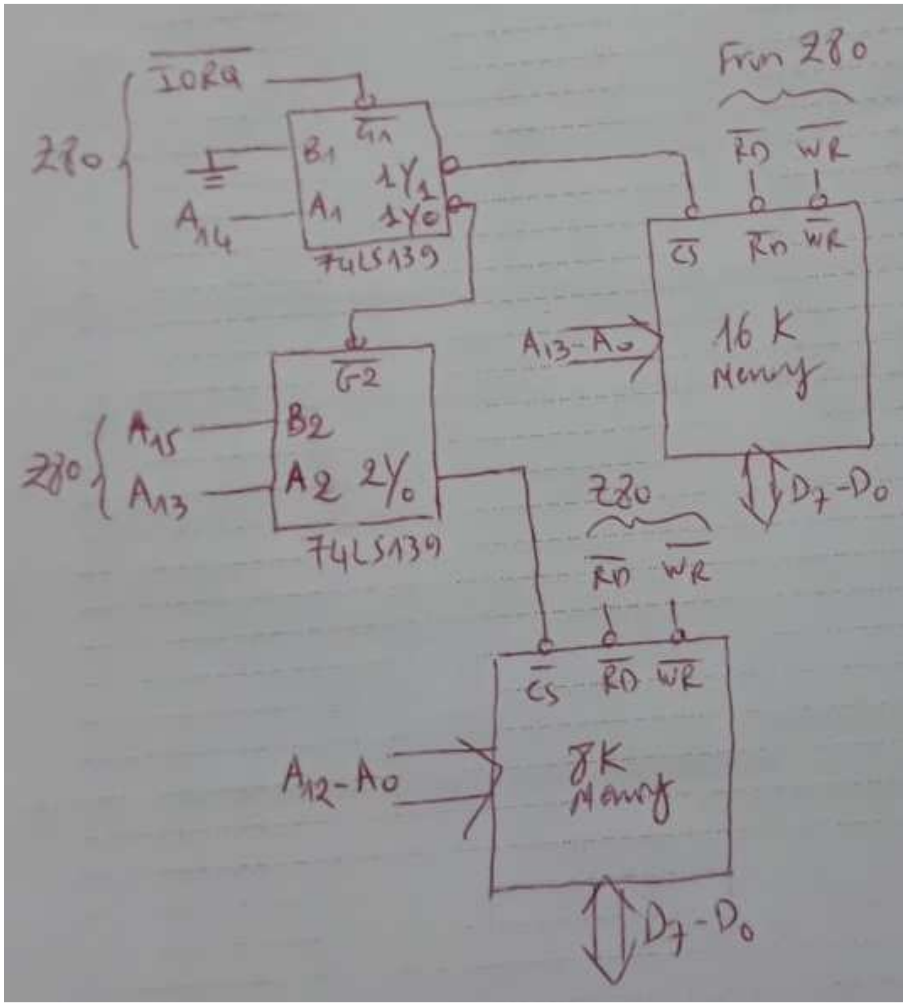
LD A, 9FH
LD (4000H), A

3.3 Which starting addresses can be used to interface the 8 Kbytes memory?

To avoid addresses conflict, the starting address is: X0X0 0000 0000 0000
Possible starting addresses are: 0000H, 2000H, 8000H, and A000H *(1 pt)*

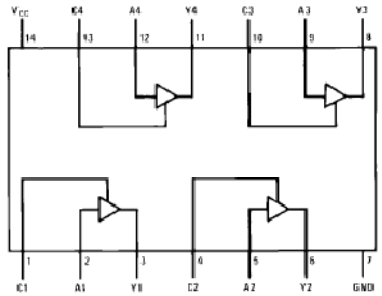
3.4 Draw the interfacing circuit using only two 2-to-4 decoder, 74LS139 contains two fully independent 2-to-4 decoder. Give the used starting address for the 8 Kbytes memory.

(2 pts)



No	Instruction	HEX code	T-states
	.ORG 2340H		
1	START: LD SP, 3FB0H	31B03FH	10
2	LD A, A9H	3EA9H	7
3	LD B, B9H	06B9H	7
4	SUB B	90H	4
5	LD (3000H),A	320030H	13
6	*HALT*	*76H*	*4*

Table 1: Simple program.

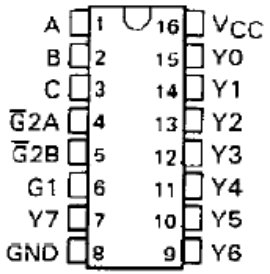


Y = A

Inputs		Output
A	C	Y
L	H	L
H	H	H
X	L	Hi-Z

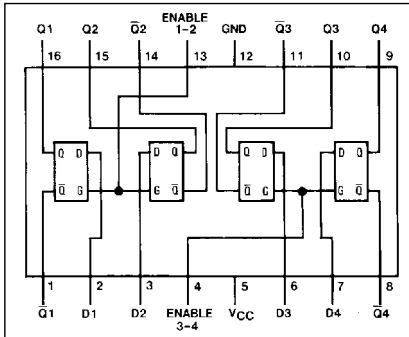
H = HIGH Logic Level
L = LOW Logic Level
X = Either LOW or HIGH Logic Level
HI-Z = 3-STATE (Outputs are disabled)

Figure 1: Pin diagram and function table of the Quad 3-state buffer (74LS126).



Inputs					Outputs							
Enable		Select										
G1	G2 (Note 1)	C	B	A	YO	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

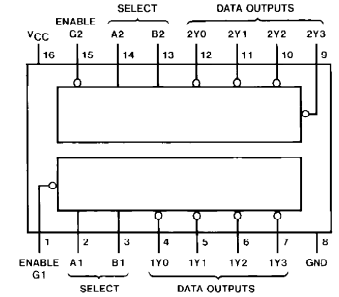
Figure 2: Pin diagram and function table of the 3-to-8 decoder (74LS138).
Note 1: $\overline{G2} = \overline{G2A} + \overline{G2B}$



Inputs		Outputs	
D	Enable	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = HIGH Level
L = LOW Level
X = Don't Care
Q_0 = The Level of Q Before the HIGH-to-LOW Transition of ENABLE

Figure 3: Pin diagram and function table of the Quad Latch (74LS75).



Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

Figure 4: Pin diagram and function table of the 74LS139 2-to-4 decoder. 74LS139 contains two fully independent 2-to-4 decoders.