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EE323: Microprocessor Systems Design
Control Solution (1h30)
2019 – 2020

Notes: Answer briefly and clearly using the provided space. No extra sheet will be accepted.

1. Z80 Assembly Program Execution (7 pts)

Consider the diagnostic routine program given in Table 1.

1.1 Give the size, the number of M-cycles, and the number of T-states of the program.

The size of the program: 7 Bytes = 56 bts
The number of M-cycles: 9 M-cycles
The number of T-states: 32 T-states

1.2 Explain the HEX code of `JR START` instruction.

18H is the opcode of JR instruction
F9H is the value of the displacement which is (-7).

1.3 How many fetch cycles, memory read cycles, and memory write cycles are executed in one loop?

Fetch cycles: 3
Memory read cycles: 4
Memory write cycle: 1

1.4 How many times Z80 inserts a) $\overline{WR}$, b) $\overline{RD}$, c) $\overline{M1}$, and d) $\overline{MREQ}$ signals in one loop?

a) $\overline{WR}$ signal: 1 time (we have one memory write cycle).
b) $\overline{RD}$ signal: 7 times (we have 3 fetch cycles and 4 memory read cycles).
c) $\overline{M1}$ signal: 3 times (we have 3 fetch cycles).
d) $\overline{MREQ}$ signal: 8 times (we have 3 fetch cycles, 4 read cycles and 1 write cycle).

1.5 Assuming 4 MHz clock frequency, give the time interval between two $\overline{WR}$ pulses.

Clock period = 1/(4MHz) = 0.25 µs
We have one $\overline{WR}$ pulse every one loop (i.e. every 32 T-states)
*Time interval = execution time of one loop = 32 * 0.25 = 8 µs*

1.6 Give the HEX value on the data bus and address bus when Z80 inserts $\overline{WR}$ signal.

Z80 inserts $\overline{WR}$ signal during the write cycle of the 2nd instruction (LD (2800H), A):
The HEX value on the data bus is: content of register A = F7H
The HEX value on the address bus is: memory address = 2800H

1.7 Give the state (low or high) of the $\overline{M1}$, $\overline{MREQ}$ and $\overline{RD}$ signals when Z80 inserts $\overline{WR}$ signals.

$\overline{M1}$ = high
$\overline{MREQ}$ = low
$\overline{RD}$ = high

2. Z80 Assembly Programming Language (7 pts)

2.1 List the different ways to specify an operand for Z80 instruction.

Immediate value, register (register-pair), memory address, and I/O.

2.2 List the different ways to specify a) source, and b) destination operand for Z80 8-bit arithmetic instructions.

a) Immediate value, register, or memory address.
b) Register A except for INC/DEC instructions, it can be any 8-bit register.

2.3 Write a simple assembly program to multiply two 8-bit unsigned numbers stored in memory locations 3000H and 3001H (Hint: $N * M = \sum_{i=1}^{M} N$). The low byte of the result should be stored at address 3002H and the high byte at address 3003H.

No	Instruction
1	`START: LD A,(3000H)`
2	`LD C,A`
3	`LD A, (3001H)`
4	`LD B,A`
5	`XOR A`
6	`LD E,A`
7	`LOOP: ADD A,C`
8	`JR NC,NOCARRY`
9	`INC E`
10	`NOCARRY: DJNZ LOOP`
11	`LD (3002H),A`
12	`LD A,E`
13	`LD (3003H),A`
14	`HALT`

2.4 A faster algorithm to multiply two 8-bit unsigned numbers is given in Figure 1. Modify the assemby program of the previous question to implement this algorithm.

No	Instruction
1	`START: LD A,(3000H)`
2	`LD C,A ; C=N`
3	`LD A, (3001H)`
4	`LD D,A ; D=M`
5	`LD B,8`
6	`XOR A ; A=LP`
7	`LD E,A ; E=HP`
8	`LOOP: ADD A,A`
9	`RL E`
10	`SLA C`
11	`JR NC,NOCARRY`
12	`ADD A,D`
13	`JR NC,NOCARRY`
14	`INC E`
15	`NOCARRY: DJNZ LOOP`
16	`LD (3002H),A`
17	`LD A,E`
18	`LD (3003H),A`
19	`HALT`
20	

3. Memory Interfacing (6 pts)

Consider memory interfacing circuit that connect Z80 to an SRAM memory chip with starting address 9400H. The memory map is 9400H-94FFH and the foldback memory ranges are: 9500-95FFH, 9600H-96FFH, and 9700H-97FFH.

3.1 What is the depth and the size of the interfaced memory? Justify.

Depth = 256 locations (from 00H to FFH)
*Size = 256*8 = 256 Bytes = 2048 bits = 2 Kbits*

3.2 What is the total used memory space? Justify.

*Used memory space = 256 *4 = 1024 bytes*

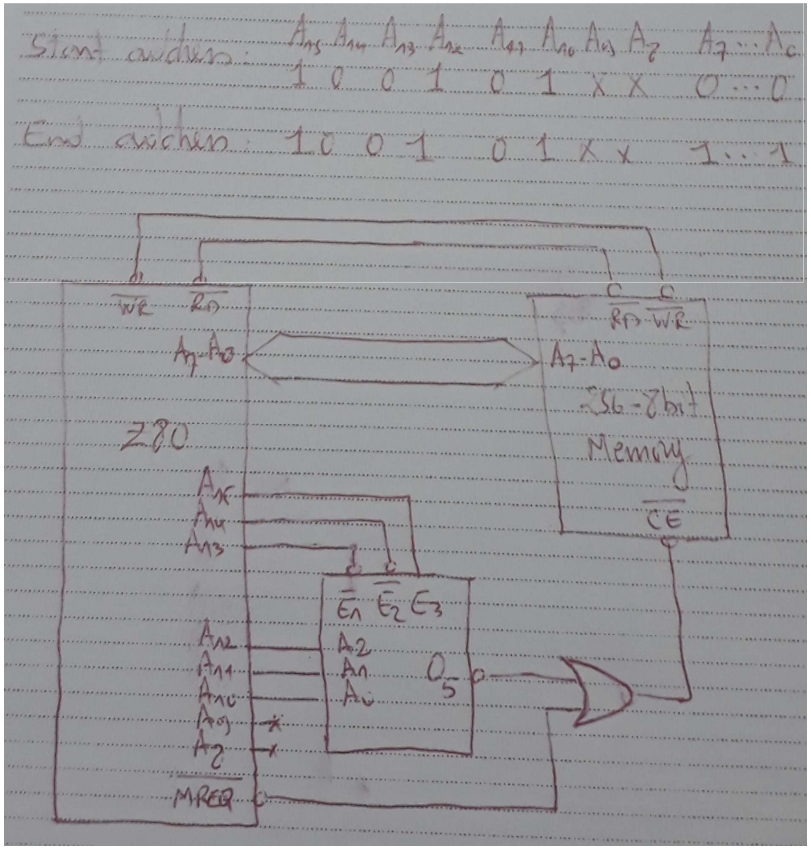
3.3 Give the Z80 addresses that can be used to point the memory location 23H.

The addresses are: 9423H, 9523H, 9623H, and 9723H

3.4 Give the "don't care" lines in the interfacig circuit.

The "don't care" address lines are A_9 and A_{10}.

3.5 Draw the interfacing circuit using 3-to-8 decoder.



Good Luck!

No	Instruction	HEX code	T-states
1	`START: LD A, 0F7H`	3EF7H	7 (4,3)
2	`LD (2800H), A`	320028H	13 (4,3,3,3)
3	*`JR START`*	*18F9H*	*12 (4,3,5)*

Table 1: Diagnostic routine.

To multiply two 8-bit unsigned numbers N and M, we can use the following equation:

$$N * M = \sum_{i=0}^{7} (n_i * 2^i * M), \quad n_i \text{ is the bit number } i \text{ of } N$$

$$N * M = n_0 * M + 2n_1M + 2^2n_2M + \cdots + 2^6n_6M + 2^7n_7M$$

$$N * M = n_0 * M + 2(n_1M + 2n_2M \ldots + 2(n_6M + 2(n_7M)))))))$$

The corresponding pseudocode is:

```
N and M are the two 8-bit unsigned numbers
LP is the low byte of the product (result)
HP is the high byte of the product (result)

BEGIN
      Initialize LP to zero
      Initialize HP to zero
      FOR i=0 to 7
            LP = LP + LP                  (i.e. LP = 2*LP)
            Rotate left HP                (i.e. HP = 2*HP + carry)
            Shift left arithmetic N       (i.e. get ni in carry flag)
            IF (carry = 1)                (i.e. if ni = 1)
                  LP = LP + M
                  IF (carry =1)           (i.e. if overflow)
                        Increment HP
END
```

Figure 1: Pseudocode for multiplication of two 8-bit unsigned numbers.

Instruction	Description
`RLC r`	The bits of register r are shifted left. The bit 7 is copied to the carry flag and to bit 0. The other bits are shifted left.
`RL r`	The bits are shifted left. The carry is copied to bit 0 and the bit 7 is copied to the carry flag.
`RRC r`	The bits are shifted right. The bit 0 is copied to the carry flag and to bit 7.
`RR r`	The bits are shifted right. The carry is copied to bit 7 and the bit 0 is copied to the carry flag.
`SLA r`	The bits are shifted left. The content of bit 7 is copied to the carry flag and '0' to bit 0.
`SRA r`	The bits are shifted right. The bit 0 is copied to the carry flag and bit 7 remains unchanged.
`SRL r`	The bits are shifted right. The bit 0 is copied to the carry flag and '0' to bit 7.

Table 2: Z80 shift and rotate instructions.