EE323: Microprocessor Systems Design
Lab. N° 3

Z80 Memory Interfacing

1 Objective

The objective of this lab is to learn how to use to interface the Z80 processor with external memory chips using full (absolute) and partial address decoding.

2 Before the Lab

1. Read "appendix I: MDA-WinZ80 Memory Circuit" of MDA-WinZ80 Manual. U1 is the Z80, U2 and U3 are memory chips 27256 and 6262 respectively, and U4 is a 3-to-8 decoder chip. Give the size and type of the U2 and U3 memory chips.
2. Which addresses are decoded by U4 chip? Give the base address for U2 and U3.
3. Why the address lines A13 and A14 of U2 are connected to the ground?
4. Explain how we can use the signals U4/x (x=7,9,10,11,12,13) available on the 50-pin external connector of the MDA-WinZ80 kit.
5. Write a program to test the memory interfacing circuit of task 2. The program should make a loop to test each memory location by comparing the writing and reading values for the location (use the two values 55H and AAH).
6. Give the complete design of the interfacing circuits of the tasks 1 and 2.

3 Lab grading

This lab is scheduled for **1 week (3 hours)** and will be graded based on:

1) Preparation.
2) Completion of the experiment, obtained results and their interpretation. During the lab, you must show the obtained results to your teacher. Before moving to a new lab experiment (task), you have to demonstrate that your implementation is working correctly, and you must show your understanding of the experiment. To evaluate your comprehension; you may have to answer oral questions.
3) Answers to the questions.
4) Attendance to the lab.
5) Report sheet.

For this lab, a report sheet will be used as lab report. You must put all your experiment results and the answers to the questions on this sheet and **return it back at the end of the lab**. When you finish a task and before moving to the next task, you should get your teacher's signature for the results of the finished task. To evaluate your comprehension, during the demonstration, you may have to answer other questions not included in the lab assignment.

4 Tasks

4.1 Task 1: Memory interfacing using partial address decoding

The objective of this task is to use partial address decoding to interface 8Kx8bit SRAM chip to the Z80 of the MDA-WinZ80 Training kit.

For the MDA-WINZ80 kit, the Z80 signals are available on the 50 pin external connector of the kit (see Figure **1**).

1) Give the memory map of the MDA-WinZ80 Training kit (see User Manual).
2) Which starting (base) addresses can be used to interface 8Kx8bit memory chip to the Z80 of the MDA-WinZ80 kit? Which starting addresses can be used to interface 64Kx8bit memory chip to the Z80 of the MDA-WinZ80 kit?
3) ***Switch OFF the power*** of the MDA-WINZ80 kit. Design and build a circuit to interface the 8Kx8bit CY6264 SRAM to the Z80 using linear address decoding (use A15=1 to select the SRAM chip). The CY6264 SRAM chip has two enable signals (one active high and one active low.
4) Instead of A15, which other address lines that can be used to avoid conflict with the already decoded addresses? Justify.
5) ***Get your circuit checked by your teacher*** before switching ON the power. Test your circuit by writing and reading different values to/from different memory locations with their foldback addresses. Give the used addresses and values.

VCC	-	1	50	- VCC
IEO	-	2	49	- VCC
U4/13	-	3	48	- U4/12
A10	-	4	47	- A11
A9	-	5	46	- A12
A8	-	6	45	- A13
A7	-	7	44	- A14
A6	-	8	43	- A15
A5	-	9	42	- CLK
A4	-	10	41	- D7
A3	-	11	40	- D6
A2	-	12	39	- D5
A1	-	13	38	- D4
A0	-	14	37	- D3
$\overline{RFSH}$	-	15	36	- D2
$\overline{M1}$	-	16	35	- D1
$\overline{RESET}$	-	17	34	- D0
$\overline{BUSRQ}$	-	18	33	- $\overline{INT}$
$\overline{WAIT}$	-	19	32	- $\overline{NMI}$
$\overline{BUSAK}$	-	20	31	- $\overline{HALT}$
$\overline{WR}$	-	21	30	- $\overline{MREQ}$
$\overline{RD}$	-	22	29	- $\overline{IORQ}$
U4/11	-	23	28	- U4/10
U4/9	-	24	27	- U4/7
GND	-	25	26	- GND

Figure 1: 50 Pin external connector of MDA-WinZ80 kit.

6) Give the different CPU addresses selecting the location 1FFFH of the SRAM.
7) ***Get your work checked by your teacher.*** Put your design on the report sheet.
8) Give the new memory map.
9) What happens if we switch two data lines (e.g. connect D_6 to I/O_7 and D_7 to I/O_6).

4.2 Task 1: Memory interfacing using full (absolute) address decoding

The objective of this task is to use full address decoding to interface 8Kx8bit SRAM chip to the Z80 of the MDA-WinZ80 Training kit.

1) Which address range is decoded by the signal U4/12 available on the 50-pin external connector of the MDA-WinZ80 kit?
2) ***Switch OFF the power*** of the MDA-WINZ80 kit. Design and build a circuit to interface the 8Kx8bit CY6264 SRAM to the Z80 using the decoded signal U4/12 as chip select signal. Give the obtained memory map.

3) Test your circuit by writing and reading different values to/from different memory locations. Give the used addresses and values.
4) ***Get your work checked by your teacher.*** Put your design on the report sheet.
5) ***Switch OFF the power*** of the MDA-WINZ80 kit. Using the 3-to-8 decoder, design and build a circuit to interface the 8Kx8bit CY6264 SRAM to the Z80 with base address A000H. Give the obtained memory map.
6) Test your circuit by writing and reading different values to/from different memory locations. Give the used addresses and values.
7) ***Get your work checked by your teacher.*** Put your design on the report sheet.
8) Is it possible to interface the SRAM to the Z80 with base address 9000H. Justify.

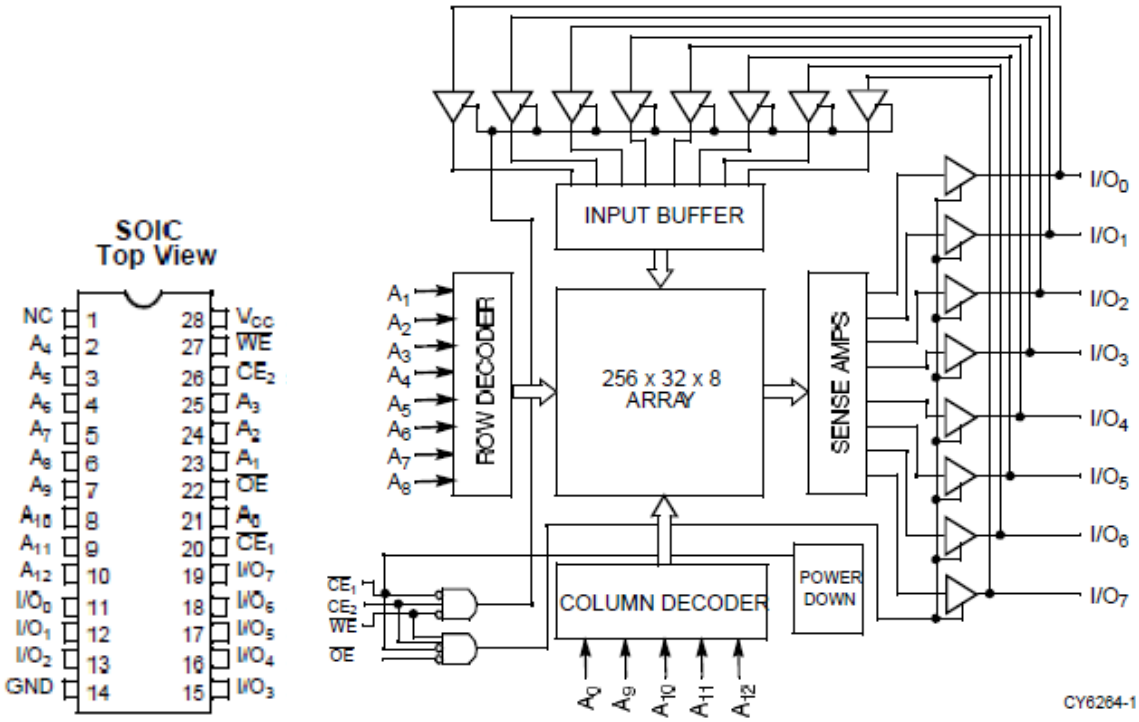
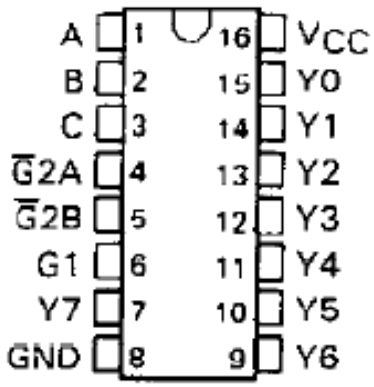


Figure 2: Pin configuration and logic block diagram of the CY6264 8Kx8bit SRAM.



Inputs					Outputs							
Enable		Select										
G1	G2 (Note 1)	C	B	A	YO	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Figure 3: Pin diagram and function table of the 3-to-8 decoder (74LS138).
Note 1: $\boldsymbol{G2} = \overline{\boldsymbol{G2A}} + \overline{\boldsymbol{G2B}}$