IGEE University M'Hamed Bougara of Boumerdès	Last Name: ..... First Name: ..... Group:	Grade :

EE321: Computer Architecture
Final Exam Solution (1h30)
2020 – 2021

Notes: Answer briefly and clearly using the provided space. No extra sheet will be accepted.

1. Basic Concepts (6 pts)

1.1 Classify as hardware or software the designs using: a) FPGA, b) Processor, c) Microcontroller, d) Integrated Circuit, and e) ASIC.

Hardware design: FPGA, IC, and ASIC
Software Design: Processor and Microcontroller. *(1 pt)*

1.2 Consider the 2's complement representation using 16 bits, complete the following equalities:

a) $(0018H)_{2'C} = (24)_{10}$ $(FFF9H)_{2'C} = (-7)_{10}$
b) $(+6)_{10} = (0006H)_{2'C}$ $(-6)_{10} = (FFFAH)_{2'C}$
(1 pt)

1.3 Give the main advantage of 2's complement representation compared to sign-magnitude representation.

The fundamental arithmetic operations are identical to those of unsigned number. *(1 pt)*

1.4 Explain the difference in the architectures of the 8-bit adder for unsigned number and for signed numbers using 2's complement representation.

It is the same architecture. *(1 pt)*

1.5 Consider an 8-bit CPU and the HEX operation: F2H-68H. Give the HEX and the decimal value of the result considering: a) unsigned numbers, and b) 2's complement representation.

a) Considering unsigned numbers: result = $(8AH)_2 = (138)_{10}$
b) Considering 2's complement representation: result = $(8AH)_{2's} = (-118)_{10}$ *(1 pt)*

1.6 Consider a sequential circuit designed using DFFs with T_{su}=29ps, T_h=12ps, and the worst propagation delay between two DFFs is 954ps. If the maximum frequency of the circuit is 865 MHz, what is the propagation delay of the DFFs?

$T_{pd}=T_{max}-T_{su}-T_{comb}=1/F_{max} - T_{su} - T_{comb} = 173$ ps. *(1 pt)*

2. Memory (7 pts)

Consider the SRAM memory of Figure 1.

2.1 Give the number of locations, the size of each location, and the size of this memory.

Number of locations: 8K = 8192 locations.
Size of each location: 8 bits
Size of the memory: 8 Kbytes = 65 536 bits

2.2 Give and justify the number of address lines used for a) row decoder, and b) column decoder.

*a) For the row decoder, we have 8 lines because we have 256*256 memory array.*
b) For column decoder, we have 5 lines because we need to select 8 bits from 256 bits.
(1 pt)

2.3 Why do we have the tristate buffers? Give and justify the number of tristate buffers.

Because the data lines are connected to a bus. We have 8-bit data bus, so we need 16 tristate buffers (input and output buffer for each data line). *(1 pt)*

2.4 Give the steps, and for each step, the values of the setted input signals to read the content of memory location 157AH.

Step 1: set $/CE_1$=0, CE_2=1, /OE=0, /WE=1, and A_{12}-A_0 = 157AH.
Step 2: read I/O_0-I/O_7. *(1 pt)*

2.5 We connect this memory to a 16-bit address bus CPU with starting address A000H, give the HEX memory location address that corresponds to the CPU address: a) B23AH and b) CF00H.

a) 123AH.
b) It does not correspond to a memory location of this memory. *(1 pt)*

2.6 Using only transistors, inverters, and multiplexers, draw the structure of a 4x1-bit SRAM (without the sense amplifier and input/output buffers.

..... *(2 pt)*

3. CPU Function and Program Execution (7 pts)

Consider a Little-Endian simple 8-bit CPU with the following specifications: 8-bit address bus, memory is byte addressable, opcodes and addressing mode codes are given in Table 1, binary codes of the general purpose registers (GPR) are given in Table 2, and the instructions format is given in Table 4. The fetch cycle takes 7 clock cycles and the read and write cycles take 3 clock cycles. The simple program given in Table 3 is stored at address A0H.

3.1 Give the number of clock cycles needed to fetch and execute the instructions: a) ML Rd X , b) LD Rd Rs, and c) AD Rd [[X]].

a) 7 clock cycles
b) 10 clock cycles
c) 13 clock cycles *(1 pt)*

3.2 Give the size and the HEX code of the given program.

*Size: 16*4=64 bits*
*HEX code: 1048604F5**03**CF**000**H (i.e. replace X by 0)*
*or: 1048604F5**FF**CF**FFF**H (i.e. replace X by 1)* *(1 pt)*

3.3 Give the content of registers MAR, MBR, IR, and PC after fetching the third instruction.

MAR =A5H
MBR =50H
IR =503CH
PC = A6H *(1 pt)*

3.4 Give the content of registers R1, R2, MBR, and PC after executing the third instruction.

R1 =F8H
R2 =XXH
MBR =50H
PC = A2H (A6H-04H) *(1 pt)*

3.5 What is the range of 2's complement value that can be specified in the instruction: a) AD Rd X, and b) JP X?

a) We have 6 bits to code the value X, so the range is [-32, 31].
b) We have 6 bits to code the displacement X, so the range is [-32, 31].

3.6 Write an assembly program to add the value -4 to the content of memory location 9AH.

```
ML R1, 0CH          ; Load FC to R1 (-4 = FCH)
MH R1, 0FH          ; Load FC to R1
ML R2, 0AH          ; Load 9A to R2
MH R2, 09H          ; Load 9A to R2
AD R1, [R2]         ; R1 = R1 + [R2] = R1 + [A9]
ST R2, R1           ; Store R1 into memory location A9
HL                  ; Halt
```
(2 pt)

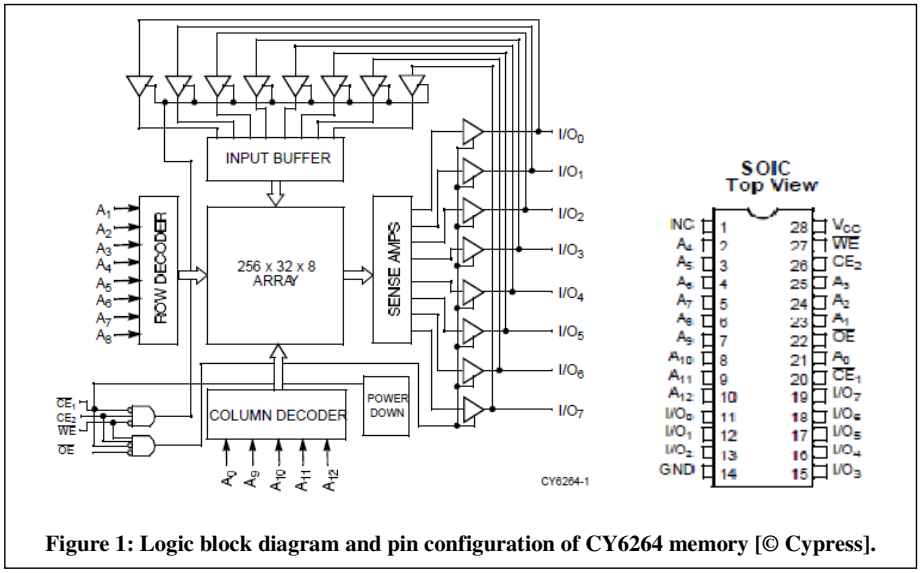

Figure 1: Logic block diagram and pin configuration of CY6264 memory [© Cypress].

Instruction	Opcode (hex)	Description	Addressing mode code (binary)
ML Rd, X	1H	$Rd_{3:0} = X_{3:0}$	000
MH Rd, X	6H	$Rd_{7:4} = X_{3:0}$	000
MV Rd, Rs	1H	Rd = Rs	001
LD Rd, [X]	2H	Rd = [X]	011
LD Rd, # Rs	2H	Rd = [R0+Rs]	101
LD Rd, Rs	2H	Rd = [Rs]	010
ST Rd, Rs	3H	[Rd] = Rs	010
AD Rd,X	4H	Rd = Rd+X	000
AD Rd, Rs	4H	Rd = Rd+Rs	001
AD Rd, [Rs]	4H	Rd = Rd+[Rs]	010
AD Rd, [X]	4H	Rd =Rd+ [X]	011
AD Rd,[[X]]	4H	Rd=Rd+[[X]]	100
AD Rd,# Rs	4H	Rd=Rd+[R0+ Rs]	101
JP X	5H	PC = PC+X	/
HL	FH	Halt	/

Rd = Source/destination register (it can be any GPR).
Rs = Source register (it can be any GPR)
R0 = Register R0. [X] = content of memory location X.

Table 1: Instructions description.

Register	Code
R0	000
R0	001
R0	010
R0	011
R0	100
R0	101
R0	110
R0	111

Table 2: Binary codes of GPRs.

No	Instruction
1	ML R1, 08H
2	MH R1, 0FH
3	JP 3CH
4	HL
5	

Table 3: Simple assembly program.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Opcode				Addressing mode			Destination register			Source operand					

Source operand can be register code, address, or 6-bit signed value. If code, bits 3 to 5 are equal to 0.
Destination register contains the binary code of source/destination register.

Table 4: Instructions format.