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EE321: Computer Architecture
Final Exam (1h30)
2019 – 2020

Notes: Answer briefly and clearly using the provided space. No extra sheet will be accepted.

1. Control Unit (9 pts)

Consider a CPU with a single accumulator AC given in Figure 1. All the arithmetic and logic instructions use the accumulator AC a source and as a destination register. The micro-operations of the fetch cycle, interrupt cycle, and execute cycle of the ADD instruction are given in Table 1.

1.1 Based on the given architecture, which registers are used for logic and arithmetic operations. Justify.

1.2 Why the first micro-operation of the execute cycle of ADD instruction is MAR←MBR(X)?

1.3 Give the micro-operations of the execute cycle of the instruction ADI (see Table 2).

1.4 Give the micro-operations of the indirect cycle and execute cycle of the ADN instruction.

1.5 We add a stack memory pointer register SP to the architecture. Give the micro-operations of the execute cycle of the PUSH and POP instruction (see Table 2).

1.6 Based on the micro-operations of the interrupt cycle, which type (vectored or non-vectored) of interrupt is implemented? Justify.

1.7 Why in Table 3, we do not have a control signal for ADN instruction?

1.8 Considering only the instructions given in Table 2 and using the control signals given in Table 3, give the boolean expression of C_8 controling the data transfer from MBR to MAR.

1.9 We assume the data transfer from SP to MAR register is controled by the control signal C_{15}. Using the control signals given in Table 3, give the boolean expression of C_{15}.

2. Instruction Set and Addressing modes (5 pts)

Consider a simple 8-bit CPU with the following specifications: 8-bit address bus, memory is byte addressable, opcodes and addressing mode codes are given in Table 4, binary codes of the general purpose registers (GPR) are given in Table 5, and the instructions format is given in Table 6.

2.1 Give the instructions that are using a direct access to the memory.

2.2 Which instructions are using a displacement mode? Give the implicit and explicit operand.

2.3 For the immediate mode, the size of the X operand is 6 bits, explain how we can load 8-bit immediate value into a register.

2.4 Give the HEX code of the instructions: a) `ML R3,08H`, b) `MH R3,0FH`, and c) `JP -7`.

2.5 Write an assembly progam to save the value 84H into memory location F6H.

3. Memory and Basic Concepts (6 pts)

3.1 Consider à 64-bit wide 2GBytes Double Data Rate 3 (DDR3 SDRAM) DIMM memory and assuming a bus clock frequency of 400MHz, give in Mbits/s, the trasfer rate of the memory.

3.2 How many 512Mx8-bit memory chips are needed to design the memory of question 3.1?

3.3 Consider the 2's complement representation using 16 bits, what is the numbers of values, the smallest and the greatest value that can be represented (give the results in decimal)?

3.4 Consider the 2's complement representation using 16 bits, give the representation of the greatest and smallest value.

3.5 Which types of trasnfer-of-control operations are implemented in Z80 processor?

3.6 Draw the CMOS schematic for the gate that implements the function: $Y = A + B(CD + C)$.

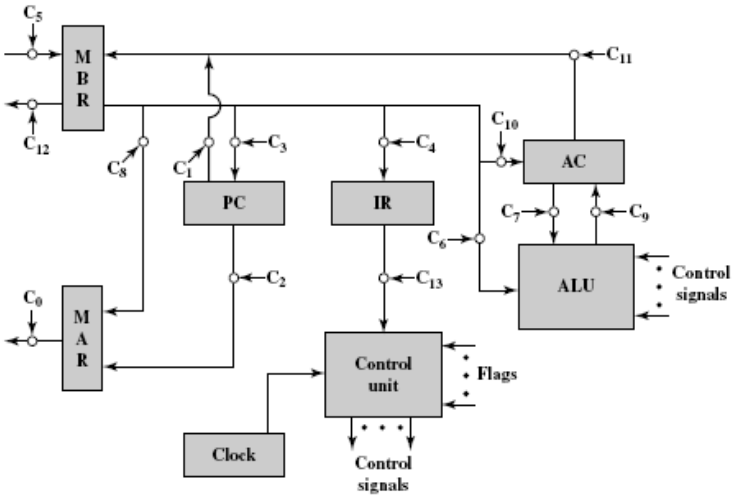

Figure 1: Data path and control signals [© Stallings].

Clock cycle	Fetch cycle	Interrupt cycle	Execute cycle of ADD instruction (i.e. ADD AC, X)
T1	*MAR ← PC*	*MBR ← PC* *MAR ← SP*	*MAR ← MBR(X)*
T2	*MBR ← Memory* *PC ← PC+1*	*Memory ← MBR* *SP ← SP+1*	*MBR ← Memory*
T3	*IR ← MBR*	*MBR ← Device*	*AC ← AC+MBR*
T4		*PC ← MBR*	
T5			

Table 1: Micro-opérations of fetch cycle, interrupt cycle, and execute cycle of the ADD instruction.

Instruction	Description
ADI AC, X	AC = AC + X
ADD AC, X	AC = AC + [X]
ADN AC, X	AC = AC +[[X]]
PUSH AC	[SP] = AC ; SP = SP +1
POP AC	SP = SP-1 ; AC = [SP]

Table 2: Instructions description for exercise 1.

Signal	Description
I	I=1 for interrupt cycle
F	F=1 for fetch cycle
E	E=1 for execute cycle
N	N=1 for indirect cycle
ADI	ADI=1 for ADI operation
ADD	ADD=1 for ADD operation
POP	POP=1 for pop operation
PUSH	PUSH=1 for push operation

Table 3: Signals used in the control unit.

Instruction	Opcode (hex)	Description	Addressing mode code (binary)
ML Rd, X	1H	$Rd_{3:0} = X_{3:0}$	000
MH Rd, X	6H	$Rd_{7:4} = X_{3:0}$	000
MV Rd, Rs	1H	Rd = Rs	001
LD Rd, [X]	2H	Rd = [X]	011
LD Rd, # Rs	2H	Rd = [R0+Rs]	101
LD Rd, Rs	2H	Rd = [Rs]	010
ST Rd, Rs	3H	[Rd] = Rs	010
AD Rd,X	4H	Rd = Rd+X	000
AD Rd, Rs	4H	Rd = Rd+Rs	001
AD Rd, [Rs]	4H	Rd = Rd+[Rs]	010
AD Rd, [X]	4H	Rd =Rd+ [X]	011
AD Rd,[[X]]	4H	Rd=Rd+[[X]]	100
AD Rd,# Rs	4H	Rd=Rd+[R0+ Rs]	101
JP X	5H	PC = PC+X	/
HL	FH	Stop the execution of the program	/

Rd = Source/destination register (it can be any GPR).
Rs = Source register (it can be any GPR)
R0 = Register R0.
X = 2's complement value.
[ ] = content of memory location.

Table 4: Instructions description for exercise 2.

Register	R0	R1	R2	R3	R4	R5	R6	R7
Code	000	001	010	011	100	101	110	111

Table 5: Binary codes of GPRs for exercise 2.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Opcode				Addressing mode			Destination register			Source operand					

Source operand can be register code, address, or value. If register code, bits 3 to 5 are equal to 0.
Destination register contains the binary code of source/destination register.

Table 6: Instructions format for exercise 2.