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EE321: Computer Architecture
Control Solution (1h30)
2019 – 2020

Notes: Answer briefly and clearly using the provided space. No extra sheet will be accepted.

1. Simple CPU Function and Structure (5 pts)

Consider a simple 16-bit CPU with the following specifications: 16-bit address bus, memory is word (2-byte) addressable, opcodes are given in Table 1, and the instruction formats are given in Table 3 and Table 4.

1.1 What is the maximum addressable memory size? Justify.

Since we have 2-byte addressable memory and 16-bit address bus, the maximum addressable memory is $16 \times 2^{16} = 1\ Mbits = 128\ KBytes$. *(1 pt)*

1.2 What is the range of the X value that can be specified in the instructions: a) LDL, b) LDH, c) ADI, and d) LDD ?

a) LDL: the size of the X operand is 8 bits, so the range is: $[-2^7, 2^7 - 1] = [-128, 127]$
b) LDH: the size of the X operand is 8 bits, so the range is: $[-2^7, 2^7 - 1] = [-128, 127]$
c) ADI: the size of the X operand is 4 bits, so the range is: $[-2^3, 2^3 - 1] = [-8, 7]$
d) LDD: the size of the X operand is 4 bits, so the range is: $[-2^3, 2^3 - 1] = [-8, 7]$

1.3 Which addressing mode is used for the instructions: a) LDL and b) LDH ?

a) LDL: Immediate addressing mode.
b) LDH: Immediate addressing mode. *(1 pt)*

1.4 Why does our simple CPU have least and most signficant bits load (LDL and LDH)?

The size of instruction is 16 bits, so we cannot load to a register a 16-bit immediate value with just one instruction. *(1 pt)*

1.5 Give the instructions size, the opcodes size, and the number of operands in an instruction.

Size of instructions: 16 bits
Size of opcodes: 4 bits
Numbers of operands: 0, 1, 2, or 3. *(1 pt)*

2. Program Execution (10 pts)

Consider the 16-bit CPU of exercise 1 with 8 GPRs (R0 to R7). We assume the program given in Table 2 is stored at address 2000H. Consider the memory content given in Table 1.

2.1 Give the size in bits of the last instruction and of the program.

The size of the last instruction: 16 *bits*
The size of the program: $6 * 16 = 96$ *bits* *(1 pt)*

2.2 Explain briefly the operation implemented by this program.

[3004H] <== [3002H] + FH *(1 pt)*

2.3 Give the memory contents (only modified locations) after the execution of the program.

The modified memory location is 3004H:
[3004H] <== [3002H] + FH = A252H + FH = A261H *(1pt)*

2.4 Give the HEX code of the program.

HEX code of the program is: 170027303172821F57420XXXH *(1 pt)*

2.5 Give the content (in HEX) of the memory that contains the program.

Address	*2000H*	*2001H*	*2002H*	*2003H*	*2004H*	*2005H*	.....	.....
Content	1700H	2730H	3172H	821FH	5742H	0XXXH	.....	*(1 pt)*

2.6 Give the HEX content of registers R1, R2, R7, MAR, MBR, PC, and IR after the execution of the fetch cycle of the 1st instruction.

R1, R2, R7 = XXXXH
MAR = 2000H
MBR = 1700H
IR = 1700H
PC = 2000H + 1 = 2001H *(1 pt)*

2.7 Give the HEX content of registers R1, R2, R7, MAR, MBR, PC and IR after the execution of the execute cycle of the 1st instruction.

R1, R2 = XXXXH
R7 = XX00H
MAR = 2000H
MBR = 1700H
IR = 1700H
PC = 2001H *(1 pt)*

2.8 Give the HEX content of registers R1, R2, R7, MAR, MBR, PC, and IR after the execution of the 5th instruction.

R1 = A252H
R2 = A261H
R7 = 3000H
MAR =3004H
MBR=A261H
IR = 5742H
PC = 2005H *(1 pt)*

2.9 What is the number of memory fetch cycles and memory read/write cycles executed by this program?

Memory fetch cycles: 6
Memory read cycles: 1
Memory write cycles: 1 *(1 pt)*

3. Digital Design Review (6 pts)

3.1 Consider the 2's complement representation using 5 bits, complete the following equalities:

a) $(01000)_{2'C} = (8)_{10}$ $(11000)_{2'C} = (-8)_{10}$
b) $(+5)_{10} = (00101)_{2'C}$ $(-6)_{10} = (11010)_{2'C}$ *(1 pt)*

3.2 Why VOH (Voltage Output High) must be greater than VIH (Voltage Input High)? What about VOL (Voltage Output Low) and VIL (Voltage Input Low)?

a) VOH must be greater than VIH to interpret correctly the high value generated by the previous gate (to have positive noise margin). (1 pt)

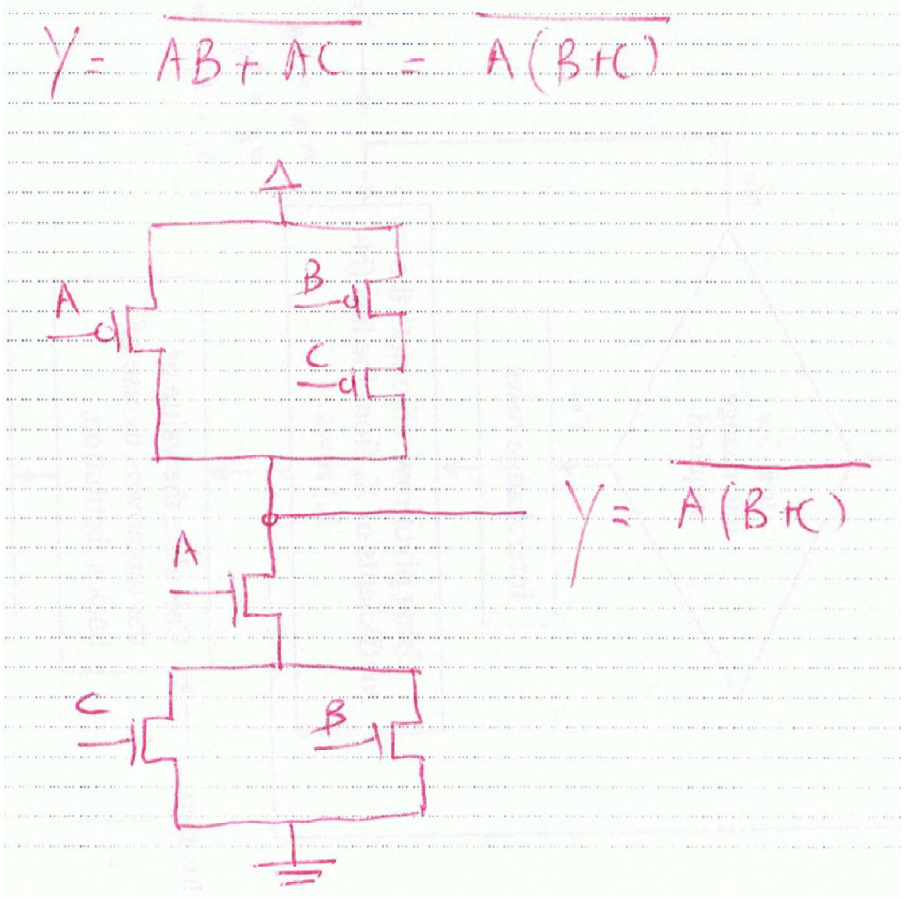
b) VIL must be greater than VOL. (1 pt)

3.3 How many MOSFET transitors we have in the CMOS gate that implements the function: $Y = \overline{AB + AC}$?

6 transistors (3 NMOS and 3 PMOS). (1pt)

3.4 Draw the CMOS transistor schematic for the gate that implements the function: $Y = \overline{AB + AC}$.

(2 pts)



Good Luck!

Instruction	Opcode	Description
LDL Rd, X	1H	Load least significant 8-bit of Rd with X ($Rd_{7:0}$ = X)
LDH Rd, X	2H	Load most significant 8-bit of Rd with X ($Rd_{15:8}$ = X)
LDD Rd, Rn,X	3H	Rd = [Rn+X]
LDR Rd, Rn,Rm	4H	Rd = [Rn+Rm]
STD Rd,X, Rn	5H	[Rd+X] = Rn
STR Rd, Rn,Rm	6H	[Rd+Rn] = Rm
ADR Rd, Rn,Rm	7H	Rd = Rn+Rm
ADI Rd,Rn,X	8H	Rd = Rn+X
ADD Rd,Rn, Rm	9H	Rd =Rn+ [Rm]
ADN Rd,Rn,Rm	AH	Rd=Rn+[[Rm]]
MVR Rd, Rn	BH	Rd = Rs
INC Rd	CH	Rd = Rd+1
HLT	0H	Stop the execution of the program

Rd = Destination register (it can be any GPR).
Rn = Source register (it can be any GPR).
Rm = Source register (it can be any GPR).
X = 2's complement value.
[ ] = content of memory location.

Table 1: Instructions description.

Instruction Number	Instruction
1	`LDL R7, 00H`
2	`LDH R7, 30H`
3	`LDD R1, R7, 2H`
4	`ADI R2, R1, FH`
5	`STD R7, 4H, R2`
6	`HLT`

Table 2: Simple program.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Opcode				1st operand				2nd operand				3rd operand			

Table 3: 3-operand instructions format.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Opcode				1st operand				2nd operand							

Table 4: Other instructions format.

Register	R0	R1	R2	R3	R4	R5	R6	R7
Code	0000	0001	0010	0011	0100	0101	0110	0111

Table 5: Binary codes of GPRs.

Address	*3000H*	*3001H*	*3002H*	*3003H*	*3004H*	*3005H*	*3006H*	*3007H*
Content	A050H	A151H	A252H	A353H	A454H	A555H	A656H	A757H

Address	*3008H*	*3009H*	*300AH*	*300BH*	*300CH*	*300DH*	*300EH*	*300FH*
Content	0018H	0119H	021AH	031BH	041CH	051DH	061EH	071FH

Table 6: Memory content.