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EE321: Computer Architecture
Control (1h30)
2019 – 2020

Notes: Answer briefly and clearly using the provided space. No extra sheet will be accepted.

1. Simple CPU Function and Structure (5 pts)

Consider a simple 16-bit CPU with the following specifications: 16-bit address bus, memory is word (2-byte) addressable, opcodes are given in Table 1, and the instruction formats are given in Table 3 and Table 4.

1.1 What is the maximum addressable memory size? Justify.

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1.2 What is the range of the X value that can be specified in the instructions: a) LDL, b) LDH, c) ADI, and d) LDD ?

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1.3 Which addressing mode is used for the instructions: a) LDL and b) LDH ?

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1.4 Why does our simple CPU have least and most signficant bits load (LDL and LDH)?

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1.5 Give the instructions size, the opcodes size, and the number of operands in an instruction.

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2. Program Execution (10 pts)

Consider the 16-bit CPU of exercise 1 with 8 GPRs (R0 to R7). We assume the program given in Table 2 is stored at address 2000H. Consider the memory content given in Table 6.

2.1 Give the size in bits of the last instruction and of the program. Justify.

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2.2 Explain briefly the operation implemented by this program.

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2.3 Give the memory contents (only modified locations) after the execution of the program.

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2.4 Give the HEX code of the program.

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2.5 Give the content (in HEX) of the memory that contains the program.

Address	.....	.....	.....	.....	.....	.....	.....	.....
Content	.....	.....	.....	.....	.....	.....	.....	.....

Address	.....	.....	.....	.....	.....	.....	.....	.....
Content	.....	.....	.....	.....	.....	.....	.....	.....

2.6 Give the HEX content of registers R1, R2, R7, MAR, MBR, PC, and IR after the execution of the fetch cycle of the 1st instruction.

2.7 Give the HEX content of registers R1, R2, R7, MAR, MBR, PC and IR after the execution of the execute cycle of the 1st instruction.

2.8 Give the HEX content of registers R1, R2, R7, MAR, MBR, PC, and IR after the execution of the 5th instruction.

2.9 What is the number of memory fetch cycles and memory read/write cycles executed by this program? Justify.

3. Digital Design Review (5 pts)

3.1 Consider the 2's complement representation using 5 bits, complete the following equalities:

$(01000)_{2'C}$ = (.....)$_{10}$ $(11000)_{2'C}$ = (.....)$_{10}$

$(+5)_{10}$ = (.....)$_{2'C}$ $(-6)_{10}$ = (.....)$_{2'C}$

3.2 Why VOH (Voltage Output High) must be greater than VIH (Voltage Input High)? What about VOL (Voltage Output Low) and VIL (Voltage Input Low)?

3.3 How many MOSFET transitors we have in the CMOS gate that implements the function: $Y = \overline{AB + AC}$? Justify.

3.4 Draw the CMOS transitor schematic for the gate that implements the function: $Y = \overline{AB + AC}$.

Good Luck!

Instruction	Opcode	Description
LDL Rd, X	1H	Load least significant 8-bit of Rd with X ($Rd_{7:0}$ = X)
LDH Rd, X	2H	Load most significant 8-bit of Rd with X ($Rd_{15:8}$ = X)
LDD Rd, Rn,X	3H	Rd = [Rn+X]
LDR Rd, Rn,Rm	4H	Rd = [Rn+Rm]
STD Rd,X, Rn	5H	[Rd+X] = Rn
STR Rd, Rn,Rm	6H	[Rd+Rn] = Rm
ADR Rd, Rn,Rm	7H	Rd = Rn+Rm
ADI Rd,Rn,X	8H	Rd = Rn+X
ADD Rd,Rn, Rm	9H	Rd =Rn+ [Rm]
ADN Rd,Rn,Rm	AH	Rd=Rn+[[Rm]]
MVR Rd, Rn	BH	Rd = Rn
INC Rd	CH	Rd = Rd+1
HLT	0H	Stop the execution of the program

Rd = Destination register (it can be any GPR).
Rn = Source register (it can be any GPR).
Rm = Source register (it can be any GPR).
X = 2's complement value.
[ ] = content of memory location.

Table 1: Instructions description.

Instruction Number	Instruction
1	`LDL R7, 00H`
2	`LDH R7, 30H`
3	`LDD R1, R7, 2H`
4	`ADI R2, R1, FH`
5	`STD R7, 4H, R2`
6	`HLT`

Table 2: Simple program.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Opcode				1st operand				2nd operand				3rd operand			

Table 3: 3-operand instructions format.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Opcode				1st operand				2nd operand							

Table 4: Other instructions format.

Register	R0	R1	R2	R3	R4	R5	R6	R7
Code	0000	0001	0010	0011	0100	0101	0110	0111

Table 5: Binary codes of GPRs.

Address	3000H	3001H	3002H	3003H	3004H	3005H	3006H	3007H
Content	A050H	A151H	A252H	A353H	A454H	A555H	A656H	A757H

Address	3008H	3009H	300AH	300BH	300CH	300DH	300EH	300FH
Content	0018H	0119H	021AH	031BH	041CH	051DH	061EH	071FH

Table 6: Memory content.