UNIVERSITE DE BOUMERDES UNIVERSITY OF BOUMERDES	*IGEE* *University M'Hamed* *Bougara of Boumerdès*	***Last Name:*** …… ***First Name:*** …… ***Group:*** ……	***Grade :***

EE321: Computer Architecture
Control (1h30)
2017 – 2018

Notes: Answer briefly and clearly using the provided space. No extra sheet will be accepted.

1. Simple CPU Function and Structure (6 pts)

Consider a simple 8-bit CPU with the following specifications: 8-bit address bus, memory is byte addressable, opcodes are given in Table 1, and the instructions format is given in Table 3.

1.1 Name the different categories of user-visible registers? What is General Purpose Register (GPR)?

1.2 What is the maximum addressable memory size? Justify.

1.3 What is the range of 2's complement value that can be specified in the MVI instruction?

1.4 Does our simple CPU have an accumulator? Justify.

1.5 Based on the given CPU specifications, what is the maximum number of GPR? Justify?

1.6 Explain why PC is incremented by 2 to point to the next instruction.

2. Program Execution (10 pts)

Consider the 8-bit CPU of exercise 1 with 8 GPRs (R0 to R7). We assume the program given in Table 2 is stored at address F0H. Consider the memory content given in Table 4.

2.1 Give the address of the first and last instruction of the program.

2.2 Which memory locations are used by this program for data read/write?

2.3 Explain in one line, the operation implemented by this program.

2.4 Give the memory contents (only modified locations) after the execution of the program.

2.5 Using the GPRs binary codes giving in Table 5, give the HEX code of the 1st instruction.

2.6 Give the content (in HEX) of the memory that contains the program.

Address	.....	.....	.....	.....	.....	.....	.....	.....
Content	.....	.....	.....	.....	.....	.....	.....	.....

Address	.....	.....	.....	.....	.....	.....	.....	.....
Content	.....	.....	.....	.....	.....	.....	.....	.....

2.7 Give the HEX content of registers R0, MAR, MBR, PC, and IR after the execution of the fetch cycle of the 1st instruction.

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2.8 Give the HEX content of registers R0, MAR, MBR, PC and IR after the execution of the execute cycle of the 1st instruction.

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2.9 Give the HEX content of registers R0, R1, R2, MAR, MBR, PC, and IR after the execution of the 5th instruction.

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3. Digital Design (4 pts)

3.1 What is the difference between Latch-D and Flip-FlopD?

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3.2 Explain operation overflow.

3.3 What is the main advantage and disadvantage of CMOS circuits compared to NMOS and PMOS circuits?

3.4 How many MOSFET transitors we have in CMOS a) NOT, b) AND, and c) NAND gates?

3.5 Draw the CMOS transistor schematic for the gate that implements the function: Y=AB+C.

Good Luck!

Instruction	Opcode	Description
MVI Rd, X	1H	Rd = X
LDD Rd, X	2H	Rd = [X]
LDP Rd, X	3H	Rd = [R0+X]
LDR Rd, Rs	4H	Rd = [Rs]
STR Rd, Rs	5H	[Rd] = Rs
ADR Rd, Rs	6H	Rd = Rd+Rs
ADM Rd,X	7H	Rd = Rd+X
ADD Rd, X	8H	Rd =Rd+ [X]
ADN Rd,X	9H	Rd=Rd+[[X]]
ADP Rd,X	AH	Rd=Rd+[R0+X]
MVR Rd, Rs	BH	Rd = Rs
HLT	FH	Stop the execution of the program

Rd = Destination register (it can be any GPR).
Rs = Source register (it can be any GPR)
R0 = Register R0.
[X] = content of memory location X.

Table 1: Instructions description.

Instruction Number	Instruction
1	`MVI R0, 10H`
2	`MVI R1, 12H`
3	*`LDD R2, 10H`*
4	*`ADP R2, 01H`*
5	*`STR R1, R2`*
6	*`HLT`*

Table 2: Simple program.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Opcode				Destination register						Source operand					

Table 3: Instructions format.

Address	Content
00H	28H
01H	29H
02H	2AH
03H	2BH
04H	2CH
05H	2DH
06H	2EH
07H	2FH

Address	Content
08H	18H
09H	19H
0AH	1AH
0BH	1BH
0CH	1CH
0DH	1DH
1EH	1EH
0FH	1FH

Address	Content
10H	08H
11H	09H
12H	0AH
13H	0BH
14H	0CH
15H	0DH
16H	0EH
17H	0FH

Table 4: Memory contents.

Register	R0	R1	R2	R3	R4	R5	R6	R7
Code	000000	000001	000010	000011	000100	000101	000110	000111

Table 5: Binary codes of GPRs.