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EE321: Computer Architecture
Final Exam Solution (1h30)
2015 – 2016

Notes: Answer briefly and clearly using the provided space. No extra sheet will be accepted.

1. Memory (7 pts)

Consider the memory block diagram given in Figure 1. We assume one square cell array.

1.1 How many bit-lines and word-lines do we have? Justify.

Square cell array => number of bit-lines = number of word-lines = 512 lines.

1.2 How many address bits are required for the row decoder? Justify.

Since we have 512 word-lines, we need 9 bits for the row decoder.

1.3 How many address bits are required for the column decoder? Justify.

Since we have 512 bit-lines and we select 4 bits for data bus, we need 7 bits for the column decoder.

1.4 If we assume the memory is designed using 8 cell arrays (2 rows by 4 colums), give the number of bit-lines and word-lines for each cell array. Justify.

Number of cells for each cell array is: 262144/8 = 32 768 cells.
Number of word-lines is: 512/2 = 256 word-lines.
Number of bit-lines is: 512/4 = 128 bit-lines.

1.5 Assuming 8 cell arrays, for each cell array, how many address bits are required for: a) row decoder, and b) column decoder? Justify.

a) *Since we have 256 word-lines, we need 8 bits for the row decoder.*
b) *Since we have 128 bit-lines and we select 1 bit for data, we need 7 bits for column decoder.*

1.6 Give the steps, and for each step, the values of the input signals (address, data, and control signals) to read the content of location 0F8AH.

Step 1: set /CS=0, /OE=1, /W=1, /RAS=0, /CAS=1, and A_7-A_0 = 8AH.
Step2: set /CS=0, /OE=0, /W=1, /RAS=1, /CAS=0, and A_7-A_0 = 0FH.
Step 3: read DO_1-DO_4.

1.7 Assume that a 128Kx32-bit main memory is built using this memory chip, find the number of the used memory chips to build the main memory. Justify.

The main memory depth is 128 K locations and the depth of the memory chip is 64 K.
The main memory data width is 32 bits and the data width for the memory chip is 4 bits, so we need 16 memory chips to built a 32-bit addressable main memory.

2. Control Unit (6 pts)

Consider the simple 12-bit CPU given in Figure 2. We assume a microprogrammed control unit.

2.1 Why microprogrammed control unit is easy to update than hardwired control unit?

For hardwired control unit, we need to change all the design, but for the microprogrammed control unit we only change the content of the control unit memory.

2.2 What is the advantage and disadvantage of horizontal microinstruction compared to vertical microinstruction?

Advantage: memory size.
Disadvantage: It needs decoder circuit

2.3 Which fields do we have in horizontal microinstruction?

Next microinstruction address field
Branch condition or next address selection field
System bus control signals field
Internal CPU control signals field

2.4 Based on the simple CPU architecture, how many bits do we need for the internal CPU control signals field? Justify.

18 bits, C9 to C0 and S7 to S0.

2.5 If we assume our control unit has 240 horizontal microinstructions, hown many bits do we need for the next microinstruction address field?

8 bits to reference the 240 microinstructions.

2.6 For next microinstruction address computation, which signals are used for condition bits?

ALU flags.

3. Program Execution (7 pts)

Consider the simple 12-bit CPU given in Figure 2. The CPU has 12-bit address bus and supports the opcodes given in Table 2. The micro-operations of the fetch cycle, interrupt cycle, and execute cycle of the ADR instruction are given in Table 1. The binary codes of the general purpose registers (GPR) are given in Table 4, and the instruction format of the data processing operation is given in Table 5.

3.1 How many instructions and how many GPR can this processor support? Justify.

Since we have 4 bits for the opcode, the maximum number of instructions is 16.
Since the instruction format use 4 bits to specify GPR, the maximum number of GPR is 16.

3.2 Give the hex code of the instruction: a)**HLT**, b) **ADR AC,R0**, and c) **LDP R0,0FH**. Justify.

*a) Opcode of HLT is FH, the hex code of the instruction is **FXXH**.*
*b) Opcode of ADR is 6H, code of AC is: 7H, hex code of R0 is 0H, the hex code of the instruction is: **670H**.*
*c) Opcode of LDP is 3H, hex code of R0 is: 0H, source operand is FH, the HEX code of the instruction is: **30FH**.*

3.3 How many memory locations we can address using instruction: a) **LDI Rd,X**, b) **LDD Rd,X**, c) **LDP Rd,X**, and d)**MV Rd,Rs**? Justify.

a) No memory access.
b) Since we have 4 bits for the address, the addressing space is $2^4 = 16$ locations.

c) Since we have 12 bits for the address, the addressing space is $2^{12} = 4K$ locations.
d) No memory access. (1)

3.4 For the **MV Rd,Rs** instruction, why: a) Rd can be any GPR except AC, and b) Rs can be any GPR except IR and MAR?

a) The internal data bus is connected to the input of AC register.
b) The output of IR and MAR registers are not connected to the internal data bus.

3.5 Consider the memory content given in Table 3. Fill the following table with the contents of the registers after the execution of the instruction stored at address 803H. Put X if unknown.

Hex code at address 803H is A73H, the instruction is ADP AC,3H
AC = AC + [R0+X] = AC + [80AH + 3H] = AC + [80D] = 001H + F11H = F12H

Register	AC	PC	MBR	MAR	IR	R0	R1	R2	R3
Before	001H	803H	X	X	X	80AH	809H	808H	807H
After	F12H	804H	F11H	80DH	A73H	-	-	-	-

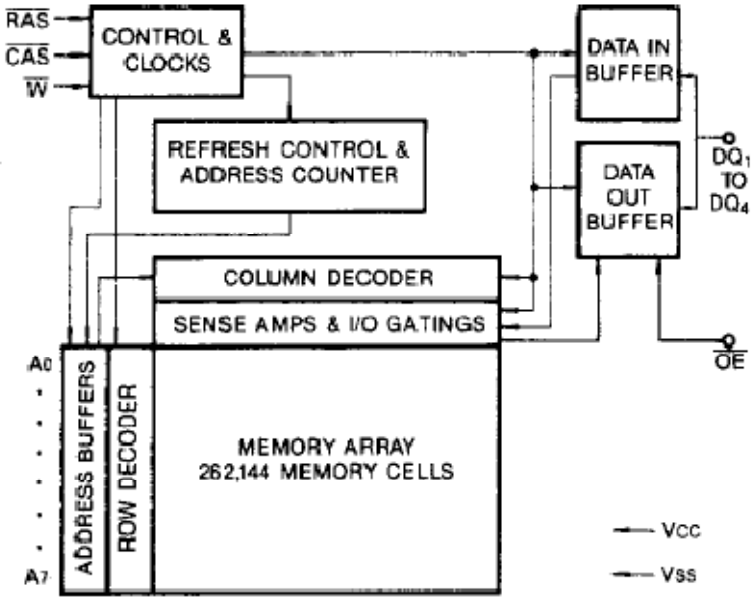
3.6 Give the micro-operations and time units for the execute cycle of the instruction stored at location 803H.

T1: MAR <-- R0+3
T2: MBR <-- data in
T3: AC <-- AC + MBR

3.7 Give the contents of the registers at each time unit of the execute cycle of the instruction stored at address 803H.

Register	AC	PC	MBR	MAR	IR	R0	R1	R2	R3
End fetch	001H	804H	A73H	803H	A73H	80AH	809H	808H	807H
T1	-	-	-	80DH	-	-	-	-	-
T2	-	-	F11H	-	-	-	-	-	-
T3	F12H	-	-	-	-	-	-	-	-

Good Luck!



Pin Name	Pin Function
A_0-A_7	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Output Enable
DQ_1-DQ_4	Data In/Out
V_{CC}	Power (+5V)
V_{SS}	Ground

Figure 1: Memory block diagram [© Samsung].

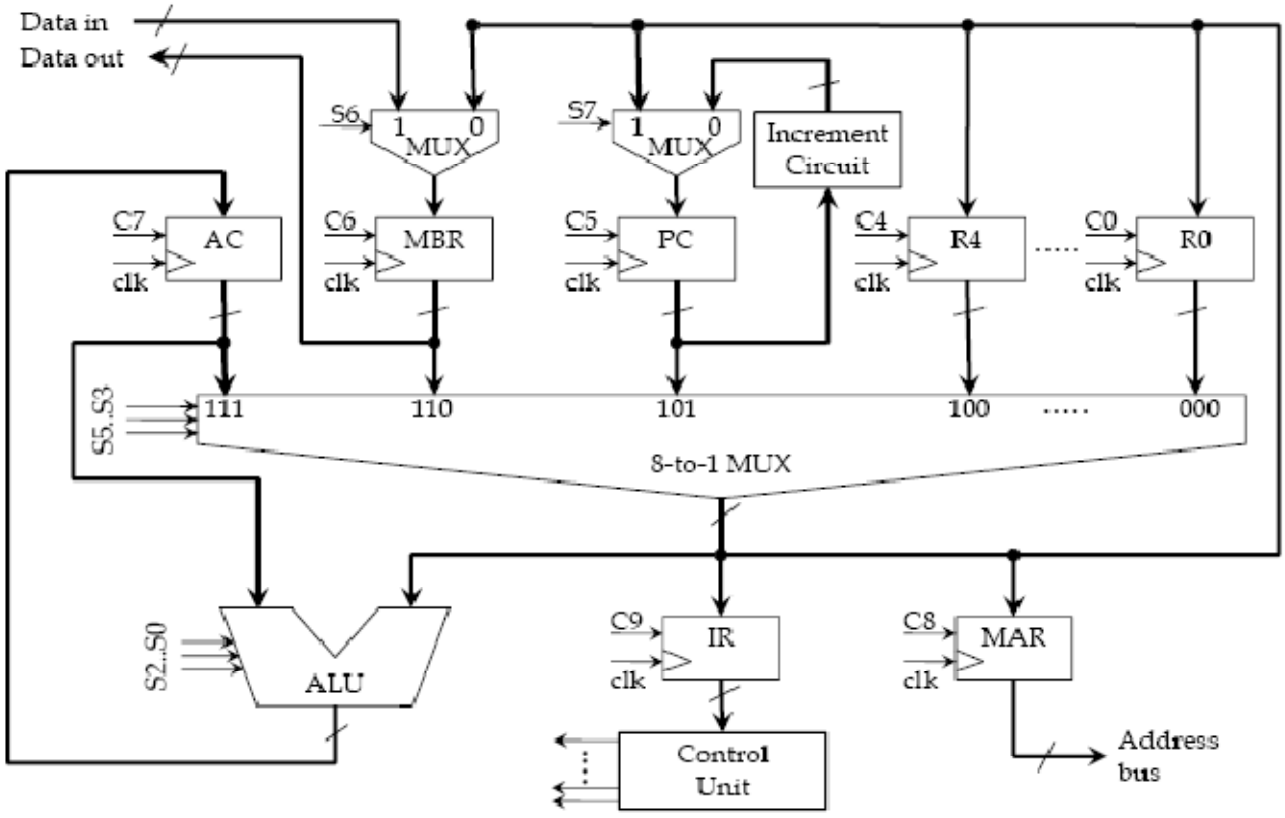


Figure 2: Simple CPU architecture.

Clock cycle	Fetch cycle	Interrupt cycle	Execute cycle of ADR instruction (i.e. ADR AC, Rs)
T1	*MAR ← PC*	*MBR ← PC*	*AC ← AC + Rs*
T2	*MBR ← data in*	*MAR ← save address*	
T3	*IR ← MBR* *PC ← PC+1*	*Memory ← MBR* *PC ← ISR address*	

Table 1: Micro-opérations of fetch cycle, interrupt cycle, and execute cycle of the ADR instruction.

Instruction	Opcode	Description
LDI Rd, X	1H	Rd = X
LDD Rd, X	2H	Rd = [X]
LDP Rd, X	3H	Rd = [R0+X]
LDR Rd, Rs	4H	Rd = [Rs]
STR Rd, Rs	5H	[Rd] = Rs
ADR AC, Rs	6H	AC = AC+Rs
ADM AC,X	7H	AC = AC+X
ADD AC, X	8H	AC =AC+ [X]
ADN AC,X	9H	AC=AC+[[X]]
ADP AC,X	AH	AC=AC+[R0+X]
MV Rd, Rs	BH	Rd = Rs
HLT	FH	Stop the execution of the program

Rd = Destination register (it can be any GPR except AC).
Rs = Source register (it can be any GPR except IR and MAR)
R0 = Register R0.
AC = Accumulator.
[X] = content of memory location X.

Table 2: Instructions description.

Address (hex)	Content (hex)
800H	10FH
801H	21EH
802H	32AH
803H	A73H
804H	B37H
805H	543H
806H	F05H
807H	F06H
809H	F07H
80AH	F08H
80BH	F09H
80CH	F10H
80DH	F11H
80EH	F02H
80FH	F03H

Table 3: Memory Content

Register	R0	R1	R2	R3	R4	PC	MBR	AC	IR	MAR
Code	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001

Table 4: Binary codes of GPR.

11	10	9	8	7	6	5	4	3	2	1	0
Opcode				Destination register				Source operand			

Source operand can be register or value.
Destination register is the register used to save the result of the operation.

Table 5: Data processing instruction format.