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| | ***IGEE***<br>***University M'Hamed***<br>***Bougara of Boumerdès*** | ***Last Name:*** ……<br>***First Name:*** ……<br>***Group:*** …… | ***Grade :*** |

***EE321: Computer Architecture***
***Control (1h30)***
***2016 – 2017***

**Notes: Answer briefly and clearly using the provided space. No extra sheet will be accepted.**

## 1. Simple CPU Function and Structure (14 pts)

Consider the simple 12-bit CPU given in Figure 1 with the following specifications:

- 12-bit address bus.
- The instruction format provides 4 bits for the opcode and 8 bits for the operands.

1.1 Give the size of data registers, instruction register, program counter, and memory address register. Justify

1.2 How many total registers does our simple CPU have? Justify.

1.3 What is the maximum addressable locations? Justify.

1.4 What is the maximum addressable memory size? Justify.

1.5 Does our simple CPU have accumulator? Justify.

1.6 Which signal is the intenal data bus? What is its size?

1.7 Which of the registers R0 to R9 is a) program counter, b) memory buffer register, c) memory address register, and d) instruction registser? Justify.

1.8 What is the function of the increment circuit?

1.9 Based on the simple CPU architecture, which signals are generated by the control unit?

1.10 Based on the simple CPU architecture, give the micro-operations and time units for fetch cycle.

1.11 Give the active control signals for each micro-operation of fetch cycle.

1.12 Give the microoperations and time units for execute cycle of **MV Rd,Rs** instruction given in Table 1.

1.13 Give the microoperations and time units for execute cycle of **ADD Rd,Rs** instruction given in Table 1.

1.14 Give the microoperations and time units for execute cycle of **STR Rd,Rs** instruction given in Table 1.

## 2. Interrupt cycle (6 pts)

Consider the micro-operations of the interrupt cycle given in Table 2.

2.1 What is save_address?

2.2 What is ISR_address?

2.3 Is-it possible to combine micro-operations 1 and 2 in the same clock cycle? Justify.

2.4 Is-it possible to combine micro-operations 3 and 4 in the same clock cycle? Justify.

2.5 Consider a maskable interrupt of Z80 processor and the following data and register values: A=00H, F=10H, PC=F00H, IR=0F00, SP=00F0H, I= 0FH, R=F0H, and data bus=03H. Give the value of save_address and ISR_address in case of a) interrupt mode 1, and b) interrupt mode 2.

***Good Luck!***

| Instruction | Opcode (Hex) | Description |
|---|---|---|
| LDI Rd, X | 1H | Rd = X |
| LDD Rd, X | 2H | Rd = [X] |
| LDP Rd, X | 3H | Rd = [R0+X] |
| LDR Rd, Rs | 4H | Rd = [Rs] |
| STR Rd, Rs | 5H | [Rd] = Rs |
| ADR Rd, Rs | 6H | Rd = Rd+Rs |
| ADM Rd,X | 7H | Rd = Rd+X |
| ADD Rd, X | 8H | Rd =Rd+ [X] |
| ADN Rd,X | 9H | Rd=Rd+[[X]] |
| ADP Rd,X | AH | Rd=Rd+[R0+X] |
| MV Rd, Rs | BH | Rd = Rs |
| HLT | FH | Stop the execution of the program |

*Rd = Destination register (it can be any GPR).*
*Rs = Source register (it can be any GPR)*
*R0 = Register R0.*
*[X] = content of memory location X.*

**Table 1: Instructions description.**

| Clock cycle | MOP Nb. | Micro-operation (MOP) |
|---|---|---|
| T1 | *1* | *MBR ← PC* |
| T2 | *2* | *MAR ← save_address* |
| | *3* | *PC ← ISR_address* |
| T3 | *4* | *Memory ← MBR* |

**Table 2: Micro-opérations for interrupt cycle.**

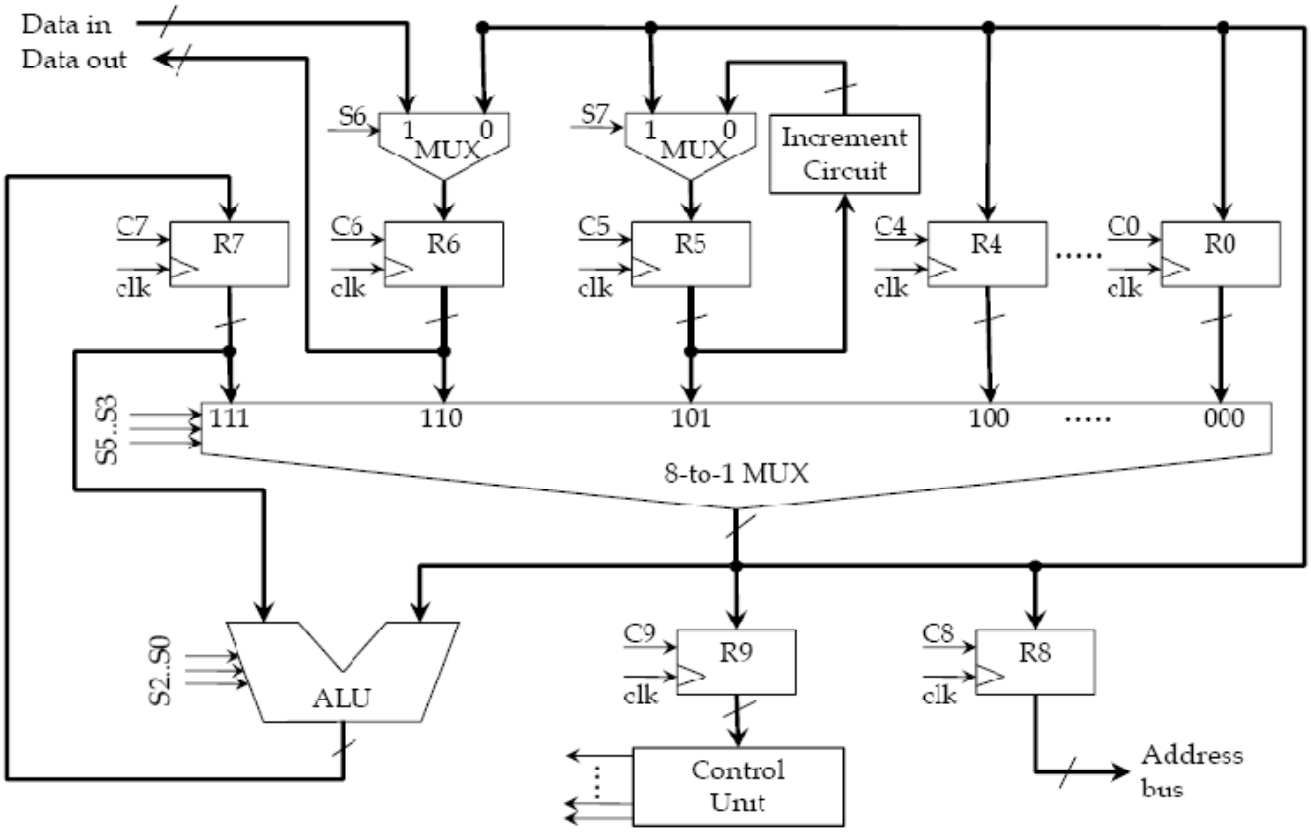


**Figure 1: Simple CPU architecture.**