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EE321: Computer Architecture
Final Exam Solution (1h30)
2015 – 2016

Notes: Answer briefly and clearly using the provided space. No extra sheet will be accepted.

1. Memory (8 pts)

Consider the memory block diagram given in Figure 1.

1.1 Is this memory dynamic or static? Justify.

It is a DRAM memory, because it has sense amps and a refresh blocks.

1.2 Give the size of this memory. Justify.

Since we have 262144 cells, the size is $262144\ bits = 2^{18} bits = 256\ Kbits$

1.3 Give the data width of this memory. Justify.

Since we have 4 data input/output pins, the memory data width is 4 bits.

1.4 Find the depth (number of memory locations) of this memory. Justify.

Since the memory data width is 4 bits, we have: $\frac{262144}{4} = 64K\ locations$

1.5 How many bits are required to address all the memory locations? Justify.

Since the memory depth is 64K, we need 16 bits for the address ($2^{16} = 64K$).

1.6 How many address pins in this memory chip? Explain the difference in the number of bits.

There are 8 address pins instead of 16, the memory use address multiplexing.

1.7 How many locations do we need to save a 16-bit 2's complement value?

Since the memory data width is 4 bits, we need 4 locations to save a 16-bit data.

1.8 The first locations (statrting at location 0) holds a 16-bit 2's complement code for -511 decimal value. Assuming big-endian memory, give the addresses and contents of the memory locations holding this value. Justify.

$(-511)_{10} = (FE01)_{2's complement}$ *, so the contents of the memory locations are:*

Address (Hex)	*0000*	*0001*	*0002*	*0003*
Content (Hex)	*F*	*E*	*0*	*1*
Content (binary)	*1111*	*1110*	*0000*	*0001*

1.9 Assume that a 1Mbits main memory is built using this memory chip and that the main memory is 4-Byte addressable (data width= 4 Bytes). Find the number of the used memory chips to build the main memory. Justify.

The main memory depth is 32 K locations and the depth of the memory chip is 64 K.
The main memory data width is 32 bits and the data width for the memory chip is 4 bits, so we need 8 memory chips to built a 4-Byte addressable main memeory, but only half of the chip memory locations will be used.

2. Control Unit (6 pts)

Consider a CPU with an accumulator AC and the internal data bus given in Figure 2. All the arithmetic and logic instructions use the registers AC and Y as sources and AC as destination. The micro-operations of the fetch cycle, interrupt cycle, and execute cycle of the ADD instruction are given in Table 1.

2.1 Based on the micro-operations of the ADD instruction, which addressing mode is used for this instruction? Justify.

Since a part of the IR is used as an address of the operand, the ADD instruction use direct addressing mode.

2.2 Give the micro-operations of the execute cycle of the add instruction using the immediat mode (i.e. ADI AC, X).

T1: $Y \leftarrow X$ *; (X = IR (address))*
T2: $Z \leftarrow AC + Y$
T3: $AC \leftarrow Z$

2.3 Give the micro-operations of the execute cycle of the add instruction using the indirect mode (i.e. ADIN AC, X).

T1: $MAR \leftarrow X$ *; (X = IR (address))*
T2: $MBR \leftarrow Memory$
T3: $Y \leftarrow MBR$
T4: $Z \leftarrow AC + Y$
T5: $AC \leftarrow Z$

2.4 Assuming a 100 Mhz clock frequency, calculate the execution time of each of the following instructions: a)ADI, b)ADD, and c)ADIN. Justify.

a) 6 clock cycles (3 for the fetch cycle and 3 for the execute cycle) --> 60 ns
b) 8 clock cycles (3 for the fetch cycle and 5 for the execute cycle) --> 80 ns
c) 10 clock cycles (3 for the fetch cycle and 7 for the execute cycle) --> 100 ns

2.5 Assuming only the add operations and using the control signals given in Table 2, give the boolean expression of the control signals: a) C1 controling the data transfert from the internal bus into the MBR, b) C2 controling the data transfer from the MBR to the internal bus, and c) C3 controling the data transfer between the MBR and the external bus. Justify.

a) *C1 is active only in interrupt cycle (at T1)*
$==> C_1 = I \cdot T_1$
b) *C2 is active in fetch cycle (at T3), and execute cycle for direct mode (at T3) and indirect mode (at T3 and T5)*
$==> C_2 = F \cdot T_3 + E \cdot ADD \cdot (\overline{M_1} \cdot M_0 \cdot T_3 + \cdot M_1 \cdot \overline{M_0} \cdot (T_3 + T_5))$
c) *C3 is active in fetch cycle (at T2), interrupt cycle (at T3), and execute cycle for direct mode (at T2) and indirect mode (at T2 and T4)*
$==> C_3 = F \cdot T_2 + I \cdot T_3 + E \cdot ADD \cdot (\overline{M_1} \cdot M_0 \cdot T_2 + M_1 \cdot \overline{M_0} \cdot (T_2 + T_4))$

3. Instruction Set (6 pts)

Consider a 16-bit CPU with 16-bit address bus and 16-bit data bus. The CPU supports the instructions given in Table 3. The binary codes of some general purpose registers (GPR) are given in Table 4. The instruction formats of the data processing operations are given in Table 5.

3.1 How many instructions and how many GPR can this processor support? Justify.

Since we have 5 bits for the opcode, the maximum number of instructions is 32.
Since the instruction formats use 3 bits to specify GPR, the maximum number of GPR is 8.

3.2 Give the addressing modes for the following instructions: ADI, ADC, ADP and ADR?.

ADI: Indirect mode.
ADC: Direct mode.
ADP: Displacement (indexed) mode.
ADR: Register mode.

3.3 Which field is implicit and which one is explicit in the displacement mode? Jusitfy.

Register R0 is explicit, because it is not coded in the instruction.
Displacement X is explicit.

3.4 How many memory locations can this processor address using: a) direct addressing, b) indirect addressing, and c) register addressing? Justify.

a) *Since we have 8 bits for the address, the addressing space is $2^8 = 256$ locations.*
b) *Since we have 16-bit address bus, the addressing space is $2^{16} = 65\,536$ locations.*
c) *Data is in the register; this mode does not have an effective address, no memory location addressing.*

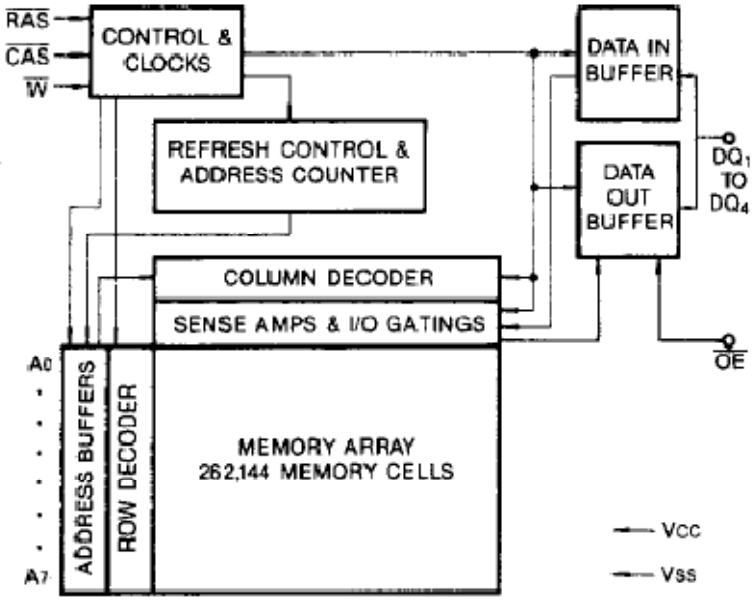
3.5 Considering 2's complement fixed-point representation Q4 (i.e. 4 bits for the fractional part), what is the range of the value that can be specified using: a) immediate addressing, b) direct addressing, and c) register addressing?

a) *Since we have 8 bits to code the value, we have 4 bits for the integer part and 4 bits for the fractional part. The range is [-8.0, 7.9375]*
b) *Since we have 16 bits, we have 12 bits for the integer part and 4 bits for the fractional part. The range is [-2048.0, 2047.9375]*
c) *Since we have 16 bits, the range is [-2048.0, 2047.9375]*

3.6 Give the HEX code of the instructions: a) ADR R1,R2, and b) ADP R1,0FH. Justify.

a) *Opcode of ADR is: 10000, binary code of R1 is: 001, binary code of R2 is 010, binary code of the instruction is: 1000 0001 1111 1010, the HEX code of the instruction is: 81FAH.*
b) *Opcode of ADP is: 10011, binary code of R1 is: 001, binary code of 0F is 00001111, binary code of the instruction is: 1001 1001 0000 1111, the HEX code of the instruction is: 990FH.*

Good Luck!



Pin Name	Pin Function
A_0-A_7	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Output Enable
DQ_1-DQ_4	Data In/Out
V_{CC}	Power (+5V)
V_{SS}	Ground

Figure 1: Memory block diagram [© Samsung].

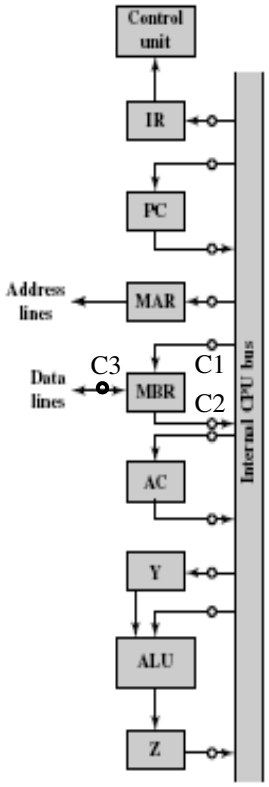


Figure 2: Internal data bus [© Stallings].

Clock cycle	Fetch cycle	Interrupt cycle	Execute cycle of ADD instruction (i.e. ADD AC, X)
T1	*MAR ← PC*	*MBR ← PC*	*MAR ← IR(X)*
T2	*MBR ← Memory* *PC ← PC+1*	*MAR ← address* *PC ← ISR address*	*MBR ← Memory*
T3	*IR ← MBR*	*Memory ← MBR*	*Y ← MBR*
T4			*Z ← AC + Y*
T5			*AC ← Z*

Table 1: Micro-opérations of fetch cycle, interrupt cycle, and execute cycle of the ADD instruction.

Signal	Description
I	Interrupt signal, I=1 for interrupt cycle
F	Fetch signal, F=1 for fetch cycle
E	Execute signal, E=1 for execute cycle
ADD	Add signal, ADD=1 for add operations
M_1M_0	Addressing mode signals, M_1M_0=00 for immediate mode, 01 for direct mode, and 10 for indirect mode

Table 2: Signals used in the control unit.

Instruction	Opcode	Nb. of cycles	Description
LDI Rd, X	00001	4	Rd = X
LDD Rd, X	00010	7	Rd = [X]
LDP Rd, X	00011	7	Rd = [R0+X]
LDR Rd, Rs	00100	7	Rd = [Rs]
STR X, Rs	01010	7	[X] = Rs
ADR Rd, Rs	10000	4	Rd = Rd+Rs
ADD Rd,X	10001	4	Rd = Rd+X
ADC Rd, X	10010	7	Rd =Rd+ [X]
ADI Rd,X	10011	10	Rd=Rd+[[X]]
ADP Rd,X	10011	10	Rd=Rd+[R0+X]
MV Rd, Rs	00111	4	Rd = Rs
HLT	11111	4	Stop the execution of the program

Rd = Destination register (it can be any GPR).
Rs = Source register (it can be any GPR)
R0 = GPR number 0.
[X] = content of memory location X.

Table 3: Instructions description.

Register	R0	R1	R2	R3
Code	000	001	010	011

Table 4: Binary codes of some GPR.

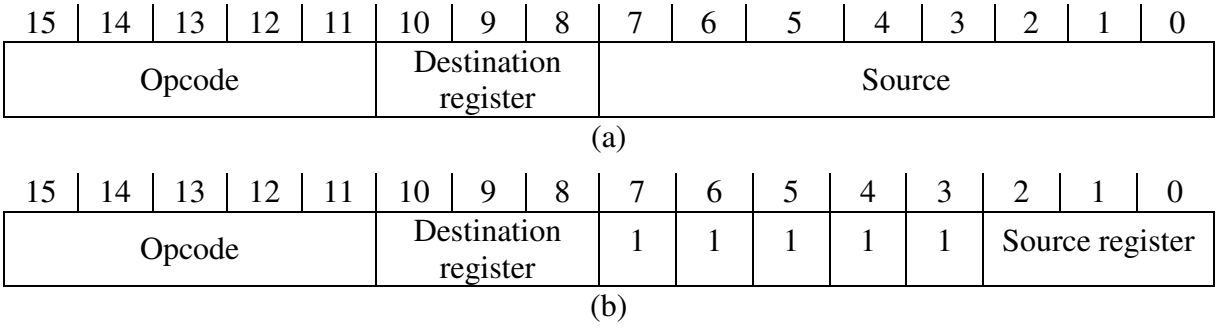


Table 5: Data processing instruction format for: a) Immediate, direct, indirect, and displacement addressing modes, and b) register and register indirect addressing modes.