UNIVERSITE DE BOUMERDES UNIVERSITY OF BOUMERDES	*IGEE* *University M'Hamed* *Bougara of Boumerdès*	*Last Name:* ..... *First Name:* ..... *Group:*	*Grade :*

EE321: Computer Architecture
Final Exam (1h30)
2015 – 2016

Notes: Answer briefly and clearly using the provided space. No extra sheet will be accepted.

1. Memory (8 pts)

Consider the memory block diagram given in Figure 1.

1.1 Is this dynamic or static memory? Justify.

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1.2 What is the size of this memory? Justify.

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1.3 What is the data width of this memory? Justify.

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1.4 Find the depth (number of memory locations) of this memory. Justify.

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1.5 How many bits are required to address all the memory locations? Justify.

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1.6 How many address pins the memory chip has? What do you notice? Explain.

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1.7 How many locations do we need to save a 16-bit 2's complement value into this memory?

1.8 The first locations (statrting at location 0) holds a 16-bit 2's complement code for -511 decimal value. Assuming big-endian memory, give the addresses and contents of the memory locations holding this value. Justify.

1.9 Assume that a 1Mbits main memory is built using this memory chip and that the main memory is 4-Byte addressable (data width= 4 Bytes). Find the number of the memory chips thar are used to build the main memory. Justify.

2. Control Unit (6 pts)

Consider a CPU with an accumulator AC and the internal data bus given in Figure 2. All the arithmetic and logic instructions use the registers AC and Y as sources and AC as destination. The micro-operations of the fetch cycle, interrupt cycle, and execute cycle of the ADD instruction are given in Table 1.

2.1 Based on the micro-operations of the ADD instruction, which addressing mode is used for this instruction? Justify.

2.2 Give the micro-operations of the execute cycle of the add instruction using the immediat addressing mode (i.e. ADIM AC, X).

2.3 Give the micro-operations of the execute cycle of the add instruction using the indirect addressing mode (i.e. ADIN AC, X).

2.4 Assuming a 100 Mhz clock frequency, calculate the execution time of each of the following instructions: a)ADD, b)ADIM, and c)ADIN. Justify.

2.5 Assuming only the add operations and using the control signals given in Table 2, give the boolean expression of the control signals: a) C1 controling the data transfert from the internal bus into the MBR, b) C2 controling the data transfer from the MBR to the internal bus, and c) C3 controling the data transfer between the MBR and the external bus. Justify.

3. Instruction Set (6 pts)

Consider a 16-bit CPU with 16-bit address bus and 16-bit data bus. The CPU supports the instructions given in Table 3. The binary codes of some general purpose registers (GPR) are given in Table 4. The instruction formats of the data processing operations are given in Table 5.

3.1 How many instructions and how many GPR can this processor support? Justify.

3.2 Give the addressing mode for the following instructions: ADI, ADC, ADP and ADR?.

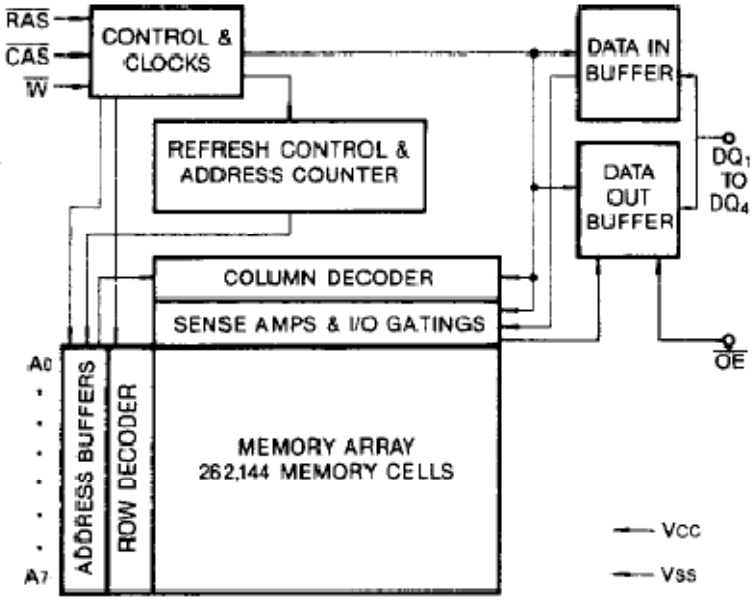
3.3 Which field is implicit and which one is explicit in the displacement mode? Jusitfy.

3.4 How many memory locations can this processor address using: a) direct addressing, b) indirect addressing, and c) register addressing? Justify.

3.5 Considering 2's complement fixed-point representation Q4 (i.e. 4 bits for the fractional part), what is the range of the value that can be specified using: a) immediate addressing, b) direct addressing, and c) register addressing?

3.6 Give the HEX code of the instructions: a) ADR R1,R2, and b) ADP R1,0FH. Justify.

Good Luck!



Pin Name	Pin Function
A_0-A_7	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Output Enable
DQ_1-DQ_4	Data In/Out
V_{CC}	Power (+5V)
V_{SS}	Ground

Figure 1: Memory block diagram [© Samsung].

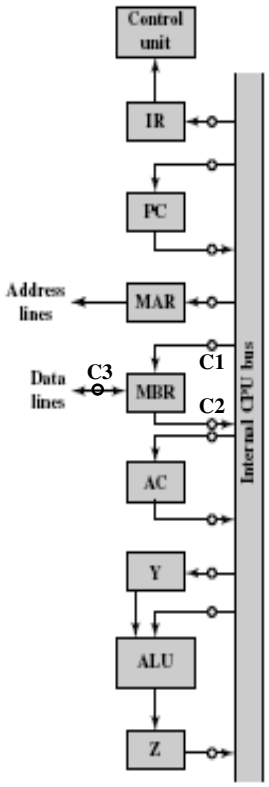


Figure 2: CPU Internal data bus [© Stallings].

Clock cycle	Fetch cycle	Interrupt cycle	Execute cycle of ADD instruction (i.e. ADD AC, X)
T1	*MAR ← PC*	*MBR ← PC*	*MAR ← IR(X)*
T2	*MBR ← Memory* *PC ← PC+1*	*MAR ← Save address* *PC ← ISR address*	*MBR ← Memory*
T3	*IR ← MBR*	*Memory ← MBR*	*Y ← MBR*
T4			*Z ← AC + Y*
T5			*AC ← Z*

AC: Accumulator.
Y, Z: Internal registers.
ISR: Interrupt Service Routine.

Table 1: Micro-opérations of fetch cycle, interrupt cycle, and execute cycle of the ADD instruction.

Signal	Description
I	Interrupt signal, I=1 for interrupt cycle
F	Fetch signal, F=1 for fetch cycle
E	Execute signal, E=1 for execute cycle
ADD	Add signal, ADD=1 for add operations
M_1M_0	Addressing mode signals, M_1M_0=00 for immediate mode, 01 for direct mode, and 10 for indirect mode

Table 2: Signals used in the control unit.

Instruction	Opcode	Nb. of cycles	Description
LDD Rd, X	00001	4	Rd = X
LDC Rd, X	00010	7	Rd = [X]
LDP Rd, X	00011	7	Rd = [R0+X]
LDR Rd, Rs	00100	7	Rd = [Rs]
STR X, Rs	01010	7	[X] = Rs
ADR Rd, Rs	10000	4	Rd = Rd+Rs
ADD Rd,X	10001	4	Rd = Rd+X
ADC Rd, X	10010	7	Rd =Rd+ [X]
ADI Rd,X	10011	10	Rd=Rd+[[X]]
ADP Rd,X	10011	10	Rd=Rd+[R0+X]
MV Rd, Rs	00111	4	Rd = Rs
HLT	11111	4	Stop the execution of the program

Rd: Destination register (it can be any GPR).
Rs: Source register (it can be any GPR)
R0: GPR number 0.
[X]: content of memory location X.

Table 3: Instructions description.

Register	R0	R1	R2	R3
Code	000	001	010	011

Table 4: Binary codes of some GPR.

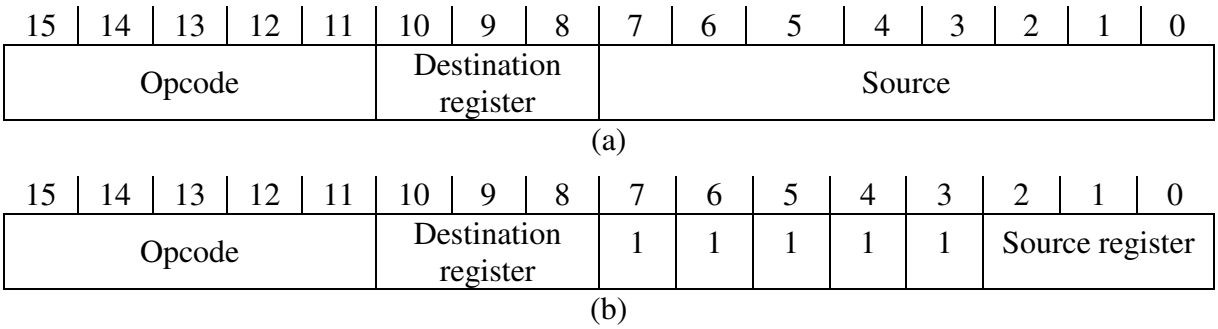


Table 5: Data processing instruction format for: a) immediate, direct, indirect, and displacement addressing modes, and b) register and register indirect addressing modes.