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EE321: Computer Architecture
Control Solution (1h30)
2015 – 2016

Notes: Answer briefly and clearly using the provided space. No extra sheet will be accepted.

1. Computer Function (4 pts)

Consider a simple CPU with the following specifications:

- Single accumulator named ACC.
- 8-bit data bus and 20-bit address bus.
- Instructions are 16 bits long and data are 8 bits long.
- The instruction format provides 4 bits for the opcode and 12 bits for the operand.

1.1 What is the maximum addressable locations?

Since we have 20-bit address bus, the maximum addressable locations is $2^{20} = 1\,048\,576\ locations = 1\ Mega\ locations$

1.2 What is the maximum addressable memory size?

Since we have 8-bit data bus, the maximum addressable memory is $8 \times 2^{20} = 8\,388\,608\ bits = 8\ Mbits = 1\ MBytes$

1.3 How many instructions can this processor support?

Since we have 4 bits for the opcode, the CPU can support $2^4 = 16\ instructions$

1.4 How many bits are needed for ACC, PC, IR, MBR, and MAR registers?

Since data are 8 bits long, ACC needs 8 bits.
Since we have 20-bit address bus, PC and MAR need 20 bits
Since instructions are 16 bits long, IR needs 16 bits
Since we have 8-bit data bus, MBR needs 8 bits

2. Program Execution (12 pts)

Consider a 16-bit CPU with 12-bit address bus, 16-bit data bus and single accumulator register named A. The CPU supports the opcodes given in table 1, the instruction format provides 4 bits for the opcode and 12 bits for the operand. Consider the memory contents of table 2.

2.1 How many bits are needed for A, PC, IR, MBR, and MAR registers?

A: 16 bits
PC: 12 bits
IR: 16 bits
MBR: 16 bits
MAR: 12 bits

2.2 What is the range of 2's complement value that can be specified in the ADI instruction?

The size of the operand is 12 bits, so the range is: $[-2^{11}, 2^{11} - 1] = [-2048, 2047]$

2.3 Write and briefly explain the corresponding assembly code of the program stored in memory location 800H.

```
1) LDD 80AH      ; Load to A the content of 80AH (i.e. A=[80AH] = 000FH)
2) MLI 010H      ; multiply A by 0010H (i.e. A=000FH<<4 = 00F0)
3) ADD 80BH      ; add the content of 80BH to A (i.e. A=00F0H+0033H=0123H)
4) STD 80CH      ; Store A at address 80CH (i.e. [80CH] = 0123H)
5) ADI 001H      ; add 1 to the accumulator (i.e. A=0124H)
6) STD 80DH      ; store A at address 80DH (i.e. [80DH] = 0124H)
7) HLT           ; stop the execution
```

2.4 What is the size of this program?

$7\ instructions \times 16\ bits = 112\ bits = 14\ Bytes$

2.5 Give the contents of registers A, MAR, MBR, PC, and IR after the execution of the fetch cycle of the first instruction.

A = ???
MAR = 800H
MBR = 080AH
IR = 080AH
PC = PC+1 = 801H

2.6 Give the contents of registers A, MAR, MBR, PC and IR after the execution of the execute cycle of the first instruction.

$A = [80AH] = 000FH$
MAR = 80AH
MBR = 000FH
IR = 080AH
PC = 801H

2.7 Give the contents of registers A, MAR, MBR, PC, and IR after the execution of the fetch cycle of the second instruction.

A = 000FH
MAR = 801H
MBR=B010H
IR=B010H
PC=PC+1=802H

2.8 Give the contents of registers A, MAR, MBR, PC and IR after the execution of the second instruction.

$A = 000FH \times 010H = 00F0H$
MAR = 801H
MBR=B010H
IR=B010H
PC=802H

2.9 Give the memory contents (only modified locations) after the execution of the program.

The modified memory locations are (see question 2.3):

Address	*Content*
80CH	*0123H*
80DH	*0124H*

3. Instruction Cycle and Interrupts (4 pts)

3.1 Consider the ADD instruction described in table 1, which of the following states are involved in this instruction: IAC, IF, IOD, OAC, OF, DO, and OS (see table 3 for states definition).

IAC, IF, IOD, OAC, OF, and DO.

3.2 Consider the ADI instruction described in table 1, which of the following states are involved in this instruction: IAC, IF, IOD, OAC, OF, DO, and OS.

IAC, IF, IOD, and DO.

3.3 Briefly explain the hard-wired interrupt.

The address of the interrupt service routine is preloaded by hardware in the CPU.

3.4 Briefly explain the differences between maskable and non-maskable interrupts.

The maskable interrupt can be disabled or delayed by the CPU.

Good Luck!

Opcode	Mnemonic	Description
0000 (0H)	LDD	Load to the accumulator the content of the memory at the address specified by the operand
1000 (8H)	LDI	Load to the accumulator the value of the operand
0001 (1H)	STD	Store the content of the accumulator at the address specified by the operand
0010 (2H)	ADD	Add the content of the memory to the accumulator
1010 (AH)	ADI	Add the value of the operand to the accumulator
0011 (3H)	MLD	Multiply the content of the memory with the accumulator
1011(BH)	MLI	Multiply the value of the operand with the accumulator
1111 (FH)	HLT	Stop execution

Table 1: Opcodes partial list.

Address	Content
800H	080AH
801H	B010H
802H	280BH
803H	180CH
804H	A001H
805H	180DH
806H	F80DH
807H	080DH

Address	Content
808H	080EH
809H	080FH
80AH	000FH
80BH	0033H
80CH	0034H
80DH	0035H
80EH	0036H
80FH	0037H

Table 2: Memory contents.

State	Definition
IAC	Instruction Address Calculation
IF	Instruction Fetch
IOD	Instruction Operation Decoding
OAC	Operand Address Calculation
OF	Operand Fetch
DO	Data Operation
OS	Operand Store

Table 3: Instruction cycle states definition.