

2. Program Execution (12 pts)

Consider a 16-bit CPU with 12-bit address bus, 16-bit data bus and single accumulator register named A. The CPU supports the opcodes given in table 1, the instruction format provides 4 bits for the opcode and 12 bits for the operand. Consider the memory contents of table 2.

2.1 How many bits are needed for A, PC, IR, MBR, and MAR registers?

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2.2 What is the range of 2's complement value that can be specified in the ADI instruction?

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2.3 Write and briefly explain the assembly code of the program stored in memory location 800H.

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2.4 What is the size of this program?

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2.5 Give the contents of registers A, MAR, MBR, PC, and IR after the execution of the fetch cycle of the first instruction.

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3. Instruction Cycle and Interrupts (4 pts)

3.1 Consider the ADD instruction described in table 1, which of the following states are involved in this instruction: IAC, IF, IOD, OAC, OF, DO, and OS (see table 3 for states definition).

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3.2 Consider the ADI instruction described in table 1, which of the following states are involved in this instruction: IAC, IF, IOD, OAC, OF, DO, and OS.

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3.3 Briefly explain the hard-wired interrupt.

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3.4 Briefly explain the differences between maskable and non-maskable interrupts.

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Good Luck!

Opcode	Mnemonic	Description
0000 (0H)	LDD	Load to the accumulator the content of the memory at the address specified by the operand
1000 (8H)	LDI	Load to the accumulator the value of the operand
0001 (1H)	STD	Store the content of the accumulator at the address specified by the operand
0010 (2H)	ADD	Add the content of the memory to the accumulator
1010 (AH)	ADI	Add the value of the operand to the accumulator
0011 (3H)	MLD	Multiply the content of the memory with the accumulator
1011 (BH)	MLI	Multiply the value of the operand with the accumulator
1111 (FH)	HLT	Stop execution

Table 1: Opcodes partial list.

Address	Content	Address	Content
800H	080AH	808H	080EH
801H	B010H	809H	080FH
802H	280BH	80AH	000FH
803H	180CH	80BH	0033H
804H	A001H	80CH	0034H
805H	180DH	80DH	0035H
806H	F80DH	80EH	0036H
807H	080DH	80FH	0037H

Table 2: Memory contents.

State	Definition
IAC	Instruction Address Calculation
IF	Instruction Fetch
IOD	Instruction Operation Decoding
OAC	Operand Address Calculation
OF	Operand Fetch
DO	Data Operation
OS	Operand Store

Table 3: Instruction cycle states definition.